2019

CMOS Receiver Design for 802.11ac Standard Using Offline Calibrated Active Inductor Based Band Pass Filter in 90 nm Technology

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CMOS RECEIVER DESIGN FOR 802.11AC STANDARD USING OFFLINE CALIBRATED ACTIVE INDUCTOR BASED BAND PASS FILTER IN 90 NM TECHNOLOGY

A Dissertation submitted in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

by

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2019
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Dec 4, 2019

I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Shuo Li ENTITLED CMOS Receiver Design for 802.11ac Standard Using Offline Calibrated Active Inductor Based Band Pass Filter in 90 nm Technology BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

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ABSTRACT

Li, Shuo. Ph.D, Department of Electrical Engineering, Wright State University, 2019. CMOS Receiver Design for 802.11ac Standard Using Offline Calibrated Active Inductor Based Band Pass Filter in 90 nm Technology

Wireless local area network is widely used in industry and people daily life. More and more mobile devices rely on this technology to perform data communication with 2.4 GHz and 5 GHz frequency band. As the development of CMOS technology is able to keep shrinking chip size and increasing circuit integration density, traditional on-chip passive inductor inefficient area consumption issue is becoming critical to receiver front end system design. In this dissertation, an active inductor-based band pass filter is studied and implemented with 90 nm technology. This active inductor design provides very small area consumption and larger quality factor compared to conventional passive circuit. Moreover, to overcome the process variation issue on active circuit during fabrication, an automatic calibration system is implemented to monitor and compensate the process variation error of band pass filter center frequency at post-fabrication phase. Also, an 802.11ac standard receiver is designed in this dissertation with active filter and Hartley image rejection architecture embedded into the system. The receiver can down-convert a 5.25 GHz signal to a 250 MHz IF signal with input power from -90 dBm to -50 dBm. The area consumption of entire receiver is expected to be smaller compared to other published works.

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Acknowledgements

First of all, I would like to express my sincere appreciation to my dissertation advisor Dr. Saiyu Ren who guide and encourage me during my master and PhD study. I wouldn't complete my research without her nurturing and support.

Besides my advisor, I would like to thank Dr. Raymond E. Siferd who shares his experience and provides a lot of valuable academic advices in my research.

I am also grateful to my committee members, Dr. Henry Chen, Dr. Marian K. Kazimierczuk, and Dr. John M. Emmert for their great academic suggestions and time. Special thanks to my defense observer, Dr. Travis E. Doom for his kindness and time.

I pursued both master and doctoral degree in Wright State University, and I had a wonderful time in these 7 years. I am not only learning knowledge in here, but also growing up and ready for the future career challenges. Many thanks to the Department of Electrical Engineering staff and students for their encouragement and selfless help.

My deepest appreciation goes to my family who are always my strong backing. Thanks to my parents Wei Li and Zirong Yu for their unparalleled love, unconditional trust, and endless patient. Thanks to my parents-in-law Qilie Zhang and Xiaohong Xu for their continued support and encouragement. Thanks to my wife Xiaomeng Zhang for her love and countless sacrifices to help me complete this dissertation. She is always my best friend, my best research partner, and my most enthusiastic cheerleader in this amazing journey.

Finally, I would like to extend my gratitude to my grandparents Yongzheng Li and Shuwei Liu. Even though they passed away before the completion of my doctoral degree, I know they would be proud of me and I will forever be grateful for the knowledge and values they indoctrinate into me.

I. Introduction

State of the art, the Wireless Local Area Network (WLAN) is widely used in high speed communication applications [1]. Unlike traditional wired Local Area Network (LAN) with fixed device locations, the WLAN provides the benefit of mobility to connected devices. People can carry their devices to anyplace in WLAN signal covered area and maintain the connection to the network. Also, WLAN is a good solution for the situation where a large number of devices potentially may connect to the network at the same time, like shopping mall or coffee house. Moreover, with the explosive growth of home intelligence products, WLAN becomes the essential technique to share information and commands to all devices, and the router can be the only equipment that needs to wire to the internet. Therefore, the receiver design for WLAN technology has been a hot topic in mobile electronics wireless communication.

1.1 History of WLAN

WLAN communication technology was first developed by University of Hawaii in 1970, and almost 30 years later, in 1997, the first standard of WLAN: 802.11 was introduced by IEEE. After then, many additional or modified standards are updated to improve the WLAN performance. The first two standards: 802.11 and 802.11b only use unlicensed 2.4 GHz frequency band for communication, and later on the 802.11a standards employed 5 GHz band to increase data transmitting speed [2]. Recently, the mobile smart devices benefit from the recent modified standards like 802.11g/n/ac with wider channel width and advanced communication techniques that allow more connections and higher speed at same time.

1.2 Compare 2.4 GHz and 5 GHz

With IEEE 802.11 standard [3], devices can use two frequency channels: 2.4 GHz and 5 GHz to transmit data. Since the 2.4 GHz frequency band is an unlicensed band and it is the first frequency band that used on WLAN technology, nearly all the devices with Wi-Fi function supports this frequency band. As shown in Table 1.2.1, there are 14 channels assigned for 2.4 GHz WLAN operating, and only 3 of them have the non-overlapping feature (channel 1, 6 and 11) [4]. Therefore, the large amount of equipment using limited number of frequency channels at 2.4 GHz make this frequency band usually very crowded and with the possibility of interference between devices. However, in latest WLAN standards, the 5 GHz technique can use up to 24 non-overlapping frequency channels shown in Table 1.2.2 to transmit data. With the less occupation density of each channel, the 5 GHz band has better connection stability due to the reduction of interference. Furthermore, 5 GHz band can provide wider channel bandwidth (up to 160 MHz with 802.11ac standard) than 2.4 GHz (maximum 40 MHz with 802.11n standard), and every channel is non-overlapping with its adjacent channels, so that a single channel at 5 GHz band can carry more information than 2.4 GHz. However, 2.4 GHz frequency band has its own advantage in signal coverage range due to the less path loss with lower frequency. As described in Eq 1.2.1, when signal propagate through certain distance d, the path loss is inversely proportional to wavelength λ, and wavelength is inversely proportional to signal frequency.

$$\text{Loss} = 20\log_{10}\frac{4\pi d}{\lambda} \tag{1.2.1}$$

Table 1.2.1 2.4 GHz WLAN Channel and Center Frequency [4]

Channel	Center Frequency (GHz)
1	2.412
2	2.417
3	2.422
4	2.427
5	2.432
6	2.437
7	2.442
8	2.447
9	2.452
10	2.457
11	2.462
12	2.467
13	2.472
14	2.484

Table 1.2.2 5 GHz WLAN Non-Overlapping Channel and Center Frequency [4]

Channel	Center Frequency (GHz)
36	5.18
40	5.19
44	5.22
48	5.24
52	5.26
56	5.28
60	5.3
64	5.32
100	5.5
104	5.52
108	5.54
112	5.56
116	5.58
120	5.6
124	5.62
128	5.64
132	5.66
136	5.68
140	5.7
144	5.72
149	5.745
153	5.765
157	5.785
161	5.805
165	5.825

1.3 Benefit of Using 802.11ac Standard

802.11ac standard was released in 2013, and it revealed channels with 80 and 160 MHz bandwidth (for example: channel 50 with center frequency of 5.25 GHz) to transmit and receive signal. The largest improvement of 802.11ac standard shows in the maximum data transmission speed and number of connections. Devices working under the new standard can allow more data transmitting at the same time than the previous standards due to the large bandwidth. Similarly, if the bandwidth assigned to single user or device keeps the same as previous standards, the 802.11ac channel accommodate more users or devices to operate at the same time. Moreover, 802.11ac channels are able to support 256-QAM (Quadrature Amplitude Modulation) [5], which also leads a better performance than old techniques. Also, 802.11ac employs MU-MIMO (Multi User Multi Input Multi Output) technique that provides a large number of access point for low-configuration Wi-Fi devices (like smart phone) connections. Thus, 802.11ac standards is good for indoor network that built for personal Wi-Fi equipment and home intelligence products.

1.4 Receiver System of Mobile Device Background Study

As described in previous sections, WLAN technology is critical to today's blooming market of mobile smart devices. The key features of mobile IC wireless communication system design include high performance, low power consumption, and area efficiency. To realize such demands, CMOS technology is a good solution as it has been widely used in Very Large Scale Integrated (VLSI) circuit implementation for several decades with its characteristics of low power, low cost and high density.

In recently published papers, many works are focusing on the receiver system design compatible with 5 GHz WLAN standard [6] [7] [8] [9]. Most of the designs also

provide the capability of using 802.11ac feature and support maximum 160 MHz channel bandwidth. Typically, the receiver front-end design for WLAN system consists of amplifiers, filters, and mixers. Based on design specifications, these circuits are designed with different techniques and architectures. Authors in [6] propose the receiver design using direct conversion architecture to minimize the image impact created by local oscillator and reduce the complexity of system implementation. Also, the current-reuse and subthreshold techniques are employed to achieve ultra-low power consumption in amplifiers and phase locked loop. In order to address the process variation of CMOS receiver design, authors in [6] also present a low noise amplifier circuit with dynamic bias control node for self-calibration. However, the penalty of this ultra-low power receiver system design is the large on-chip area consumption taken by multiple passive inductor employed in circuits. As shown in chip micrograph of [6], the passive inductors take more than 50% of the on-chip space for RF front-end system, which results in the increased cost and size of the entire design.

In reference [8] and [9] implementations, both works implement the receiver system with direct conversion architecture. The difference between these two designs to the one introduced in [6] is that both [8] and [9] employ a 1-to-N transformer to achieve the amplification function at the first stage of entire receiver design. The benefits of this architecture are reduced power consumption and increased linearity compared to the conventional active Low Noise Amplifier (LNA) design, as the passive component is famous for low noise, low power and good linearity characteristics. The authors in [9] also add a variable gain amplifier stage between LNA and mixer to adjust the gain accordingly with the input signal amplitude. This design scheme further improve the noise and linearity performance as the system can determine the best gain value based on input signal strength. Moreover, the variable gain stage allows the

system to be more tolerant of larger input power range and higher input saturation value. Nevertheless, these two works in [8] and [9] suffer the same drawback as the system proposed in [6], which is the large on-chip area used to place passive inductors. The die photograph of reference [8] indicates that the inductors take more than 80% area of the entire receiver system.

These three referenced works all employ the direct conversion architecture to eliminate image effect. However, the major issues of direct conversion system are the flicker noise and complex channel selected filter design. As the RF signal is down-converted into baseband region, the DC current flowing through circuit creates the flicker noise in active components [10]. The low pass filter after mixer stage needs to be built with good noise suppression capability and linearity, which increases the design difficulty.

Besides, all the above reported designs are completed with multiple on-chip passive inductors which results in large on-chip area consumption and low quality factor (Q). Therefore, authors in [11] [12] [13] [14] [15] build filters by using active inductor instead of passive inductor in the system. Such active inductor can offer better area efficiency along with higher quality factor and post fabrication tunability compared to conventional passive inductor.

Even though, the active inductor has many advantages in on-chip CMOS circuit design, the major issue of this technique is the process variation effect during chip fabrication. Many factors affect the accuracy of wafer production, such as temperature, pressure and doping concentrations [16]. Consequently, the electrical properties like sheet resistance and threshold voltage will be different between transistors, although they are designed to have exactly same parameters. Such parameters process variation happens on every element throughout a whole chip and it becomes more and more

critical with CMOS technology scaling down [17]. So, the practical result of the active circuit implementation is the departure of the prefabrication design performance from post fabrication performance, and in many cases, this variation is the key reason of testing failure. Thus, to successfully replace the passive inductor by active design, a post fabrication calibration system is needed to compensate the error caused by process variation.

1.5 Motivation

With the development of CMOS process, manufactories take advantage of the latest technique to scale down the communication chip size. Meanwhile, customers always want their equipment to have longer battery life and more powerful performance. Therefore, the mobile smart device must be equipped with a receiver design that operates with the newest communication standard with minimum area consumption, to save space for high capacity battery to extend device operating time. To realize these parameters, every single circuit block built on-chip should provide high performance in minimum space.

In receiver chain system, band pass filter is a key component that is designed to receive the desired signal and filter out unwanted noise. Traditionally, the band pass filter is realized by passive on-chip L-C circuit. To achieve high quality factor, low power consumption within small system area, CMOS active inductor based band pass filter is implemented to replace the passive design and save chip area [11] [18] [19] [20].

In order to make the active inductor operating with designed performance after fabrication, a built-in automatic detecting and calibrating circuit is desired for on-chip active inductor-based band pass filter application.

1.6 Objective

- Implement an active inductor-based band pass filter that can replace the passive design in receiver system design.
- Design a calibration system for active band pass filter with process variation detection and error compensation feature.
- Implement all sub-circuits that RF receiver chain needed to meet the standard of 802.11ac, while using minimum number of on-chip passive inductor to reduce the system area consumption.
- Build and simulate the receiver system with active band pass filter in CMOS 90 nm technology.

II. Receiver System Architecture

2.1 Typical Receiver Architecture for Wireless Application

The primary function of the receiver system for wireless applications is to extract the information embedded in the high frequency carrier. Thus, the receiver chain should provide sufficient gain for the RF input signal to amplify the wanted signal, while generating minimum noise. Moreover, the system must have good channel selectivity and image suppression to ensure the data input into DSP block is pure. As shown in Fig 2.1.1, a typical front end receiver includes a RF band pass filter to select the RF input signal; an LNA to amplify the weak and noisy signal; a mixer to down-convert signal to baseband or intermediate band which can be easily handled by following DSP blocks; a local oscillator source (usually made by phase locked loop) to generate desired frequency signal for carrier removal. This typical receiver design is developed into different special structures to achieve special implementation specifications, and one big category is to eliminate image rejection which is discussed in next sub-section.

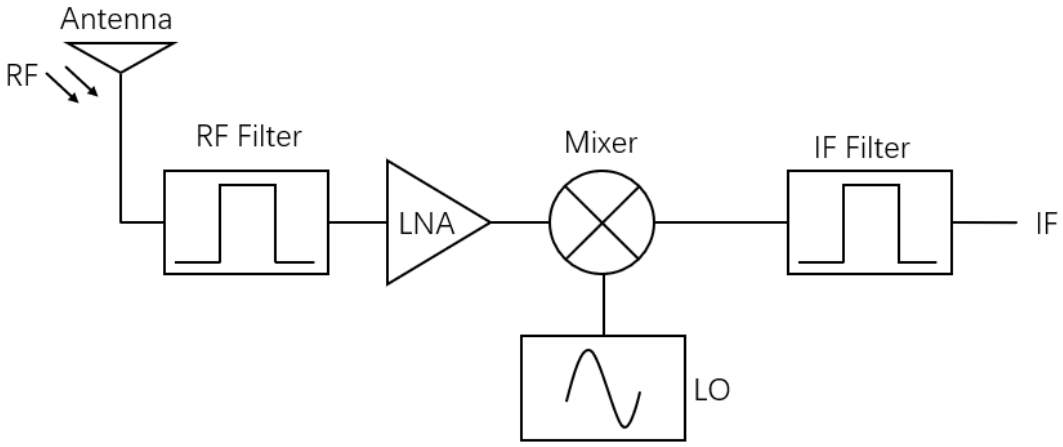

Fig 2.1.1 General architecture of receiver front end design

2.1.1 Image Rejection

Image signal is one of the vital problems of receiver system, and all the referenced works in background study section of chapter 1 did not report this parameter. The rejection of this unwanted signal can be done either in analog or digital design phases. In this dissertation, the proposed receiver system performs the image rejection feature with analog circuit design to reduce the design complexity of future digital circuit blocks.

Fig 2.1.2 demonstrates the issue existing in a receiver system, where f_{RF} is desired radio frequency input signal frequency, f_{LO} is local oscillator frequency, f_{IF} is called intermediate frequency and equals to $|f_{RF} - f_{LO}|$, f_{IM} is the image signal and its frequency is $f_{IM} = |f_{RF} - 2f_{LO}|$. Such unwanted image signal can pass through the RF input filter and overlap the f_{IF} causing degradation of wanted signal quality. To solve this issue, three different types of analog image rejection receiver architecture are widely used, and they are:

- Heterodyne receiver with image reject filter
- Hartley Architecture receiver
- Weaver Architecture receiver

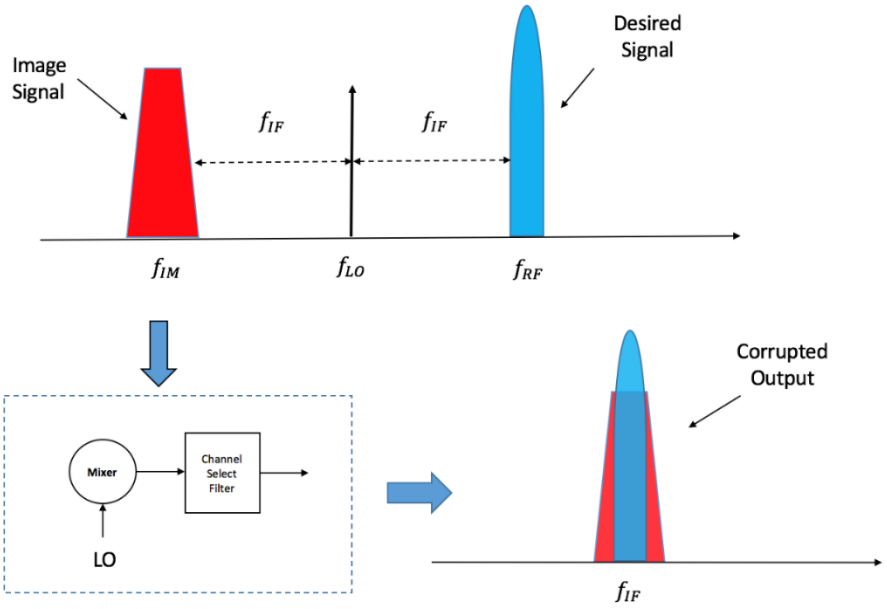

Fig 2.1.2 Image issue existing in receiver system [10]

2.1.2 Heterodyne Receiver

For Heterodyne receiver, an image reject filter is placed before mixer to eliminate the image signal and the system structure is shown in Fig 2.1.3 [21]. The benefit of this design is low complexity of the entire system. However, the drawbacks are selectivity and sensitivity of the channel select filter. The choice of f_{IF} is important. Lower f_{IF} needs high selectivity for filter, while higher f_{IF} increases design complexity of following circuitry. To solve the problem, more IF steps are needed with the help of off-chip filters resulting in increased complexity of the receiver chain.

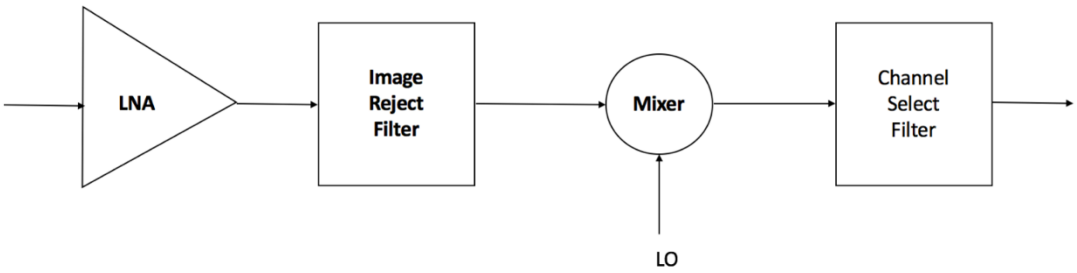

Fig 2.1.3 Heterodyne receiver architecture [21]

2.1.3 Hartley Receiver

The Low IF receiver shown in Fig 2.1.4 uses quadrature down-converting technique to clear the image signal. Theoretically, when considering both image and desired signal, the RF input can be expressed as:

$$V_{RFin}(t) = V_{RF}\cos\omega_{RF}t + V_{IM}\cos\omega_{IM}t \tag{2.1.1}$$

Where V_{RFin}, V_{RF}, and V_{IM} represent the amplitude of total input, wanted input, and image input, respectively. The ω_{RF} and ω_{IM} describe the angular velocity of wanted and image signal. After applying quadrature mixing, the down-converted signal is divided into two signals, which are:

$$V_I(t) = -\frac{V_{RF}}{2}\sin(\omega_{RF} - \omega_{LO})t + \frac{V_{IM}}{2}\sin(\omega_{LO} - \omega_{IM})t \tag{2.1.2}$$

$$V_Q(t) = \frac{V_{RF}}{2}\cos(\omega_{RF} - \omega_{LO})t + \frac{V_{IM}}{2}\cos(\omega_{LO} - \omega_{IM})t \tag{2.1.3}$$

To eliminate the image signal, Hartley architecture is proposed as illustrated in Fig 2.1.4. By employing a 90 degree shifter, $V_I(t)$ is becoming $V_I(t)$':

$$V_I(t)' = -\frac{V_{RF}}{2}\cos(\omega_{RF} - \omega_{LO})t + \frac{V_{IM}}{2}\cos(\omega_{LO} - \omega_{IM})t \tag{2.1.4}$$

Subtracting $V_I(t)$' from $V_Q(t)$ and the calibrated IF signal equals to:

$$V_{IFout}(t) = V_{RF}\cos(\omega_{RF} - \omega_{LO})t \quad (2.1.5)$$

It can be seen that Hartley architecture down-converts the RF signal to IF band without the effects of image problem. However, this approach adds the gain mismatch. If the two paths are mismatched, the image signal cannot be perfectly canceled at IF output node [22] [23].

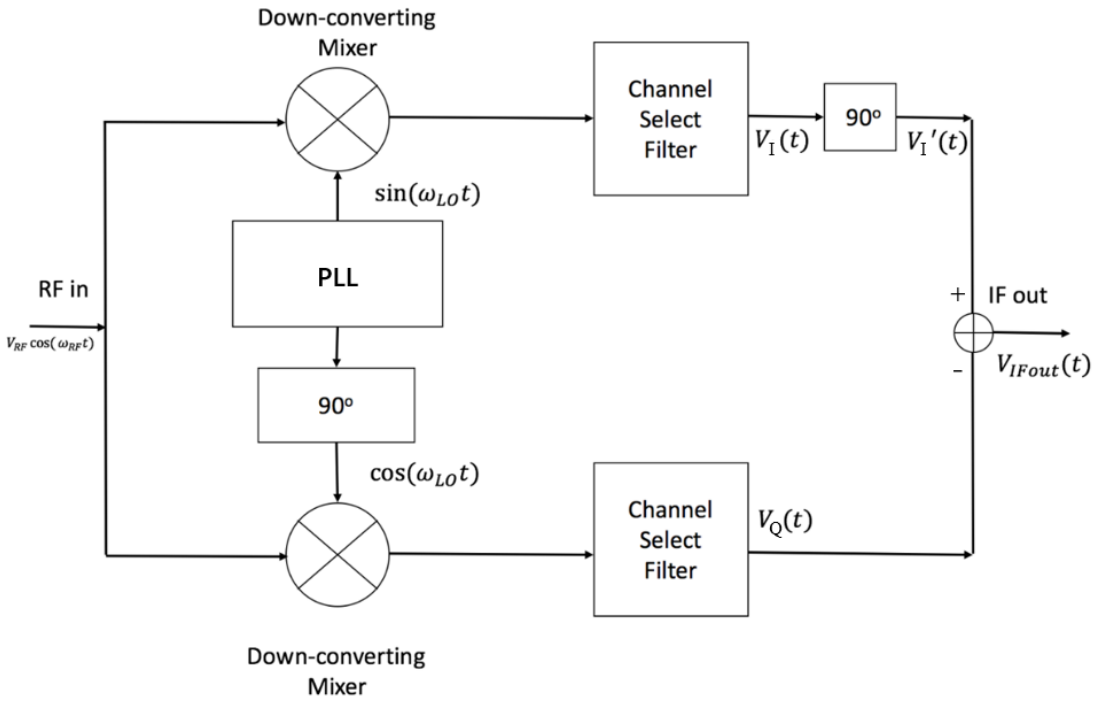

Fig 2.1.4 Hartley image rejection architecture [10]

2.1.4 Weaver Receiver

Weaver architecture is another way to eliminate the image signal, which is presented in Fig 2.1.5 [24]. The first stage mixer outputs $V_A(t)$ and $V_B(t)$ are the same as $V_I(t)$ and $V_Q(t)$:

$$V_A(t) = V_I(t) = -\frac{V_{RF}}{2}\sin(\omega_{IF1})t + \frac{V_{IM}}{2}\sin(\omega_{IM})t \quad (2.1.6)$$

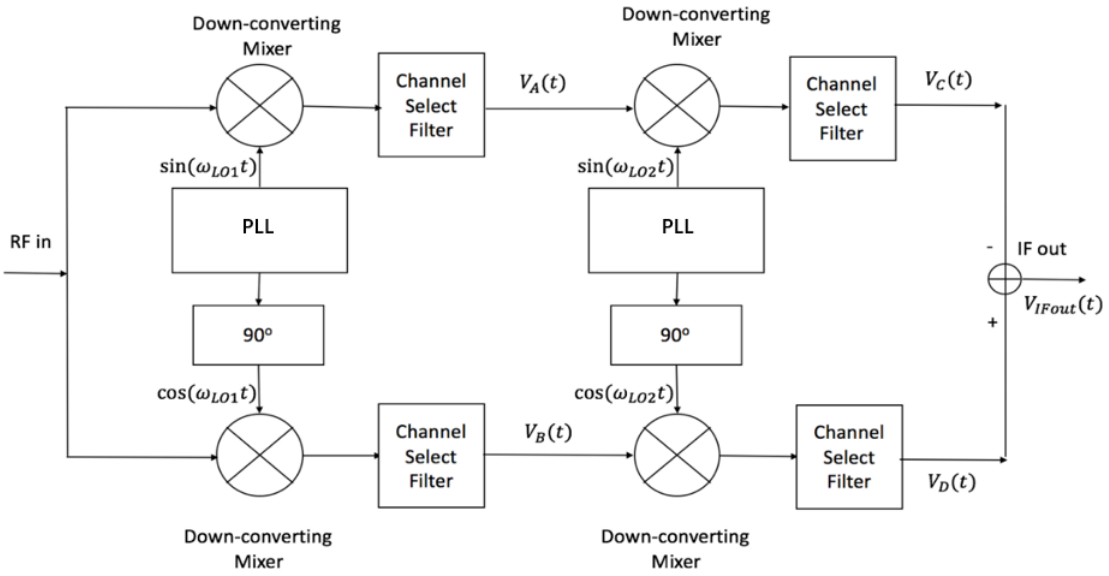

Fig 2.1.5 Weaver image rejection architecture [24]

$$V_B(t) = V_Q(t) = \frac{V_{RF}}{2}\cos(\omega_{IF1})t + \frac{V_{IM}}{2}\cos(\omega_{IM})t \tag{2.1.7}$$

After the second stage mixer, the two IF signals $V_C(t)$ and $V_D(t)$ are shifted to:

$$V_C(t) = V_A(t) \times \sin\omega_{LO2}t = -\frac{V_{RF}}{4}\cos(\omega_{IF})t + \frac{V_{IM}}{4}\cos(\omega_{IM})t \tag{2.1.8}$$

$$V_D(t) = V_B(t) \times \cos\omega_{LO2}t = \frac{V_{RF}}{4}\cos(\omega_{IF})t + \frac{V_{IM}}{4}\cos(\omega_{IM})t \tag{2.1.9}$$

And the image signal is eliminated at the output of the subtractor of $V_D(t)$ minus $V_C(t)$ as shown in Fig 2.1.5.

$$V_{IFout}(t) = V_D(t) - V_C(t) = \frac{V_{RF}}{2}\cos(\omega_{IF})t \tag{2.1.10}$$

In this dissertation, with the consideration of noise and power consumption, a low IF Heterodyne architecture combined with Heterodyne and Hartley image rejection is selected for signal processing to meet the specification of 802.11ac standard. The data path shown in Fig 2.1.6 is realized with LNA, band pass filter (also have image rejection filter feature), and Hartley quadrature down-converting system. Moreover, a Weaver system is also built and simulated to compare the performance with Hartley structure.

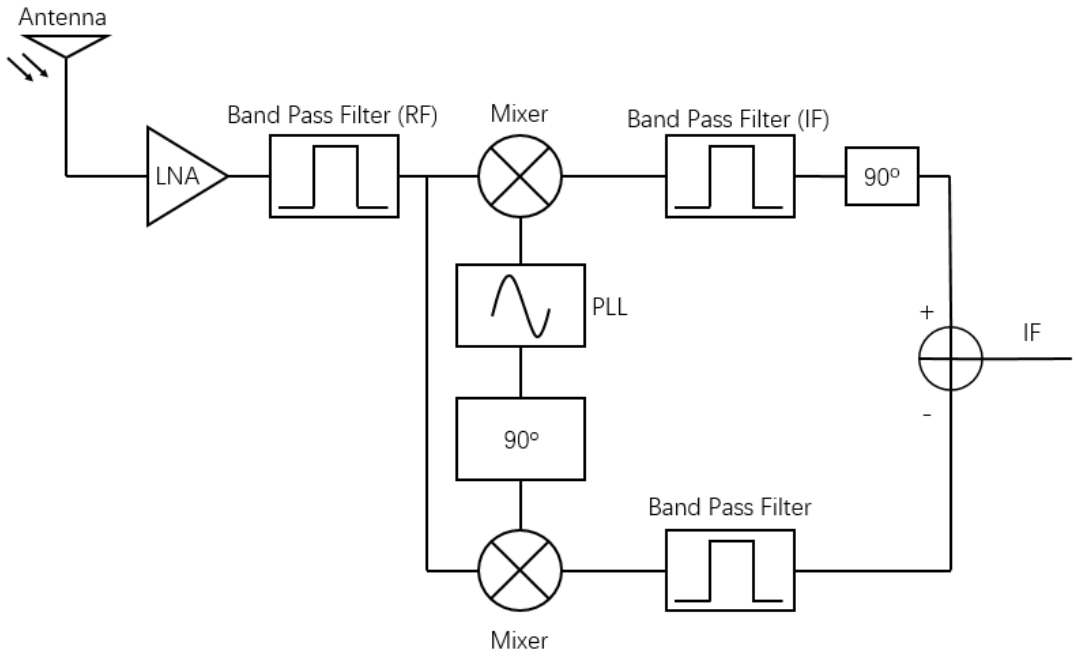

Fig 2.1.6 Proposed receiver design combined Heterodyne and Hartley architecture.

2.2 Sub-Circuits of Receiver System with Expected Performance

The main specifications of the proposed receiver system include input sensitivity, image rejection ratio, noise figure, and power consumption. With the requirement of 802.11ac standard, the minimum input sensitivity (input level) is -73 dBm, and the maximum is -30 dBm [3]. Based on power and voltage converting formula listed in Eq 2.2.1 for 50 Ω system, these number are equivalent to 70.8 uV and 10 mV in amplitude unit, respectively.

$$V_{amp} = 10^{\frac{P(dBm)-10}{20}} \tag{2.2.1}$$

Where P represent the input power and V_{amp} is the equivalent amplitude. Such RF signal needs to be processed and convert into large amplitude and low frequency IF signal which can be processed by Analog-to-Digital Converter (ADC). In this dissertation, a 9-bit ADC [25] is assumed to connect with proposed receiver chain.

Theoretically, the maximum ADC input signal amplitude is calculated as:

$$V_{ampmax} = \frac{V_{dd}-2*V_T}{2} \quad (2.2.2)$$

In 90 nm technology, V_T is approximately equal to 0.3 V, and V_{ampmax} can be estimated as 0.3 V using Eq 2.2.2. The LSB amplitude value of referred ADC is derived as:

$$V_{LSB} = \frac{V_{ampmax}}{2^N-1} \quad (2.2.3)$$

Where, N is the number of ADC bits which is 9 in the referenced work. The LSB amplitude is computed as 587 μV. In order to achieve ADC 9 bits input amplitude requirement with largest power RF input signal, and at least 2 bits with minimum input sensitivity, the entire receiver chain needs to provide approximately 30 dB gain at IF node. Moreover, the amplitude of signal injected into mixer RF input node must be large enough (in mV level) to make circuit work functionally. Therefore, the first two stages amplifier should offer sufficient gain to amplify the weak RF input signal.

The noise performance is another parameter that is very important for front end design. Eq 2.2.4 describes the noise effects on the receivers based on cascaded amplifier:

$$F = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1*G_2} + \cdots + \frac{F_N-1}{G_1*G_2*\ldots*G_{N-1}} \text{ [26]} \quad (2.2.4)$$

Noted that, in Eq 2.2.4, F is the noise factor of entire receiver chain. F_N and G_N are the noise factor and gain of N_{th} stage circuit, respectively. It can be seen that, if F_1 is small and G_1 is large, the first stage circuit dominates the entire system noise performance.

In summary, to ensure the data integrity and minimal noise impact generated from receiver system, the expected gain and noise distribution is presented in Fig 2.2.1. The

first two stages circuit should provide 30 to 40 dB gain and generate no more than 3 dB noise. Besides LNA is expected to have around 20 dB gain and less than 2 dB noise figure to guarantee the entire chain having good noise performance based on Eq 2.2.4. Since most mixer circuits are gain-loss circuit, an amplifier stage is needed to be built-in and compensate the loss. To achieve expected 30 dB signal amplification goal of entire receiver, the loss of mixer stage must be within -10 dB to 0 dB.

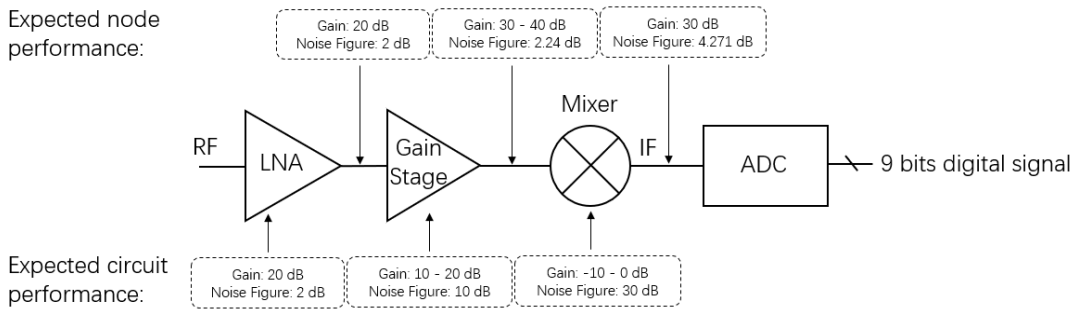

Fig 2.2.1 Receiver system expected gain and noise distribution.

III. Low Noise Amplifier

3.1 Introduction

As discussed in Chapter 2, usually a Low Noise Amplifier (LNA) is the first circuit block of a receiver chain. It amplifies the signal captured by antennas and minimizes the noise effects on the receivers. Since LNA design is so critical to the entire front-end design, it must provide reliable performance to the implementation. As well known in IC field, process variation is an unavoidable issue that can lead to performance degradation of active circuit. In this dissertation, a classic passive inductor based single ended tuned LNA shown in Fig 3.1.1 is employed with cascode and source de-generation techniques.

At input node, a gate blocking capacitor C_B and gate inductor L_G is connected in series to build the pre-select filter which can provide the lowest input power reflection (S_{11}) at targeting frequency. To amplify the signal and reduce the input capacitance introduced by Miller effect, a cascode architecture is employed in LNA design with M1 and M2 transistors. The output node inductor and varactor form a band pass filter whose resonating frequency can be tuned with bias voltage to improve the circuit gain, suppress unwanted noise, and calibrate the center frequency if LNA suffers the process variation after fabrication. Detailed circuits analysis is presented in the following sections. The goal of this design is to maximize the gain of amplifier at desired center frequency while keeping the noise at minimum level.

3.2 Theoretical Analysis

Since LNA is connected to off-chip circuit, the input node equivalent impedance should equal to general standard 50 Ω. Fig 3.2.1 demonstrates the simplified small

signal model of LNA input consisted of C_B, L_G, source inductor (L_S), and parasitic capacitor of input transistor.

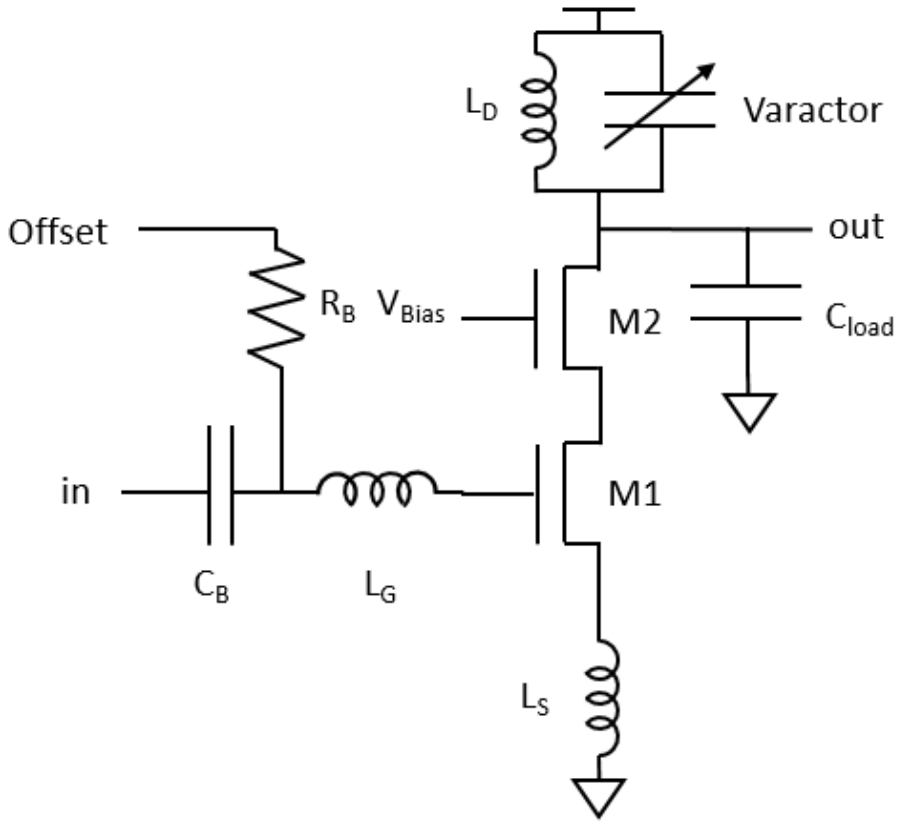

Fig 3.1.1 Schematic diagram of LNA

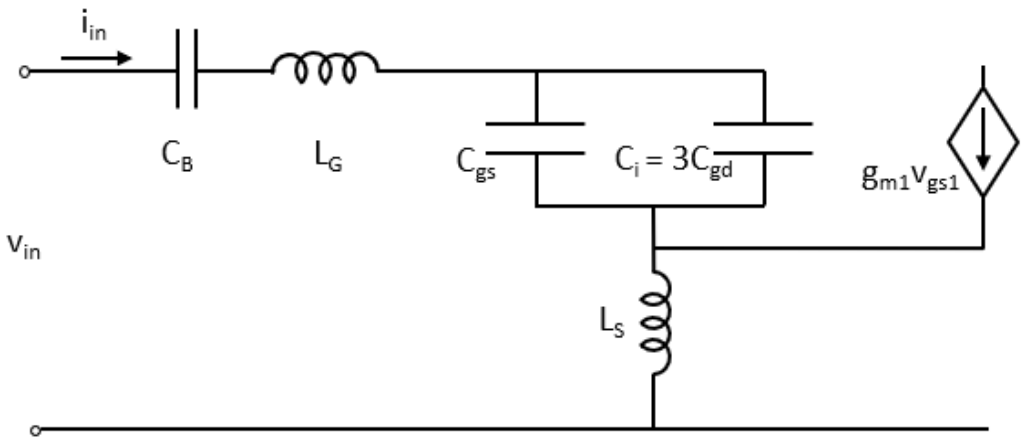

Fig 3.2.1 Small signal model of LNA input stage

In small signal model, C_{iM} is generated by input Miller effect and it can be calculated as:

$$C_{iM} = (1 - A_{v1}) * C_{gd} \text{ [27]} \tag{3.2.1}$$

It is noted that A_{v1} is the gain of first transistor and it approximately equals to -2 when M1 and M2 are the same size [27]. C_{gd} is the gate to drain capacitance of M1 transistor. Substitute A_{v1} value into Eq 3.2.1, and the Miller effect capacitance is:

$$C_i = 3C_{gd} \tag{3.2.2}$$

The equivalent input impedance based on the small signal equivalent circuit is expressed as:

$$v_{in} = (sL_G + \frac{1}{sC_B} + \frac{1}{sC_{gseq}}) * i_{in} + sL_S(i_{in} + g_{m1}v_{gs1}) \tag{3.2.3}$$

Where,

$$C_{gseq} = C_{gs} + 3C_{gd} \tag{3.2.4}$$

The input voltage of M1 transistor is:

$$v_{gs1} = \frac{i_{in}}{sC_{gseq}} \tag{3.2.5}$$

Substituting Eq 3.2.5 into Eq 3.2.3, and the equation is transformed as:

$$v_{in} = \left(sL_G + \frac{1}{sC_B} + \frac{1}{sC_{gseq}}\right) * i_{in} + sL_S\left(1 + \frac{g_{m1}}{sC_{gseq}}\right) * i_{in} \tag{3.2.6}$$

Through Eq 3.2.6, the input equivalent impedance of LNA can be calculated as:

$$Z_{in} = \frac{v_{in}}{i_{in}} = sL_G + \frac{1}{sC_B} + \frac{1}{sC_{gseq}} + sL_S\left(1 + \frac{g_{m1}}{sC_{gseq}}\right) \tag{3.2.7}$$

In order to match the off-chip 50 Ω impedance, the real component of Eq 3.2.7 should be 50 Ω, and imaginary part needs to remain zero. Therefore,

$$\frac{g_{m1}L_S}{C_{gseq}} = 50\Omega \tag{3.2.8}$$

$$s(L_G + L_S) + \frac{1}{sC_B} + \frac{1}{sC_{gseq}} = 0 \tag{3.2.9}$$

In this chapter, the following parameters are used for capacitance estimation:

$$\text{CGSO} = 0.252\,\frac{fF}{\mu m}$$

$$\text{CGDO} = 0.252\,\frac{fF}{\mu m}$$

$$C_{ox} = 12.33\,\frac{fF}{\mu m^2}$$

And,

$$C_{gseq} = C_{gs} + 3C_{gd} = \frac{2}{3}C_{ox} * W * L + \text{CGSO} * 2 * W + 3 * \text{CGDO} * W \quad (3.2.10)$$

Substituting all the constant into Eq 3.2.10, the C_{gseq} is estimated as 265 fF when width and length of M1 transistor equal to 100 μm and 200 nm respectively. The transconductance measured from proposed LNA input transistor is 3657.66 μA/V under DC operating point. Plug C_{gseq} and g_{m1} into Eq 3.2.8, source inductor L_S is estimated as 3.62 nH to make real part of input impedance match 50 ohms.

For the imaginary part, s is substituted by $j\omega_0$, and ω_0 represents angular frequency converted from designed center frequency of 5.25 GHz. Eq 3.2.9 is expressed as,

$$(L_G + L_S)\omega_0 = \frac{1}{\omega_0 C_B} + \frac{1}{\omega_0 C_{gseq}} \quad (3.2.11)$$

The sum of gate and source inductance equals to:

$$L_G + L_S = \frac{1}{{\omega_0}^2}\left(\frac{C_B + C_{gseq}}{C_B C_{gseq}}\right) \quad (3.2.12)$$

If C_B is much larger than C_{gseq}, Eq 3.2.12 becomes:

$$L_G + L_S = \frac{1}{{\omega_0}^2 C_{gseq}} \quad (3.2.13)$$

Since ω_0 equals to $2\pi*5.25*10^9$ rad/s, and C_{gseq} is calculated as 265 fF, $L_S + L_G$ is 3.84 nH based on Eq 3.2.13. The value of L_S has already been estimated as 3.62 nH, so the inductance of L_G is 220 pH.

The input impedance matching has a huge impact to LNA noise performance [28]. In this model, the gate and source inductors are placed and calculated to create 50 ohms

resistance matching with off-chip load. Matching the off chip source resistance mitigates ringing and return loss at the LNA input.

On the output node, the drain inductance can be estimated by the operating frequency and total capacitance using LC band pass filter property:

$$L_D = \frac{1}{\omega_0{}^2 C_{total}} \tag{3.2.14}$$

And,

$$C_{total} = C_{db2} + C_{gd2} + C_L \tag{3.2.15}$$

This RF band pass filter at LNA output establishes a RF input bandwidth and provides a first level of image rejection.

Assume M1 and M2 transistor in Fig 3.1.1 have the same size. The two parasitic capacitance C_{db2} and C_{gd2} are 334.75 fF and 25.2 fF, respectively. Substitute these two number and 100 fF load capacitance (include C_{load} and varactor) into Eq 3.2.15, the output node total capacitance is 459.2 fF. Plug the C_{total} into Eq 3.2.14, the drain inductance L_D is calculated as 2 nH when LNA center frequency is 5.25 GHz. This output stage band pass filter can filter out the noise out of the wanted RF signal band and also reduce the image signal impact on the entire receiver.

The above theoretical analysis describes all LNA components initial parameters that suit for 802.11ac specification. In the real circuit design, those numbers are adjusted to get the best simulation results.

3.3 Circuit Design Techniques

3.3.1 Low Threshold Voltage MOS technique

One of the benefits of using advanced CMOS technology is the decrement in power consumption due to the low supply voltage. However, the shrinking supply voltage range also limits the output signal swing especially for cascoding design shown

in Fig 3.3.1. If both transistors have the same threshold voltage V_T, the output maximum amplitude V_{outamp} is

$$V_{outamp} = \frac{V_{DD}-2V_T}{2} \quad (3.3.1)$$

Typically, the supply voltage of 90 nm is 1.2 V and threshold voltage for NMOS is approximately 0.5 V (strong on) as shown in Fig 3.3.2. Put these two numbers into Eq 3.3.1, the maximum output amplitude is only 0.1 V. In order to increase the voltage range at output node, low threshold voltage MOSFET is used in this design to mitigate stacking threshold issue. Based on Fig 3.3.2 simulation result, the low threshold voltage NMOS (lvtnfet) can be conducted at 0.4 V (strong on). Substitute this threshold voltage into Eq 3.3.1 along with 1.2V supply voltage, the output signal amplitude can reach 0.2 V which is twice of the value calculated with normal NMOS.

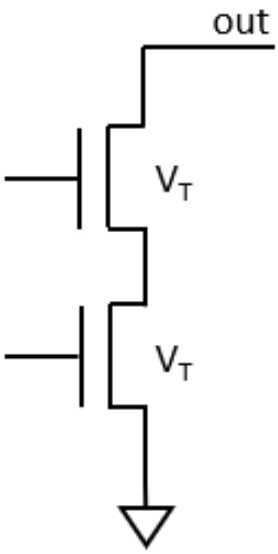

Fig 3.3.1 MOSFET cascoding model

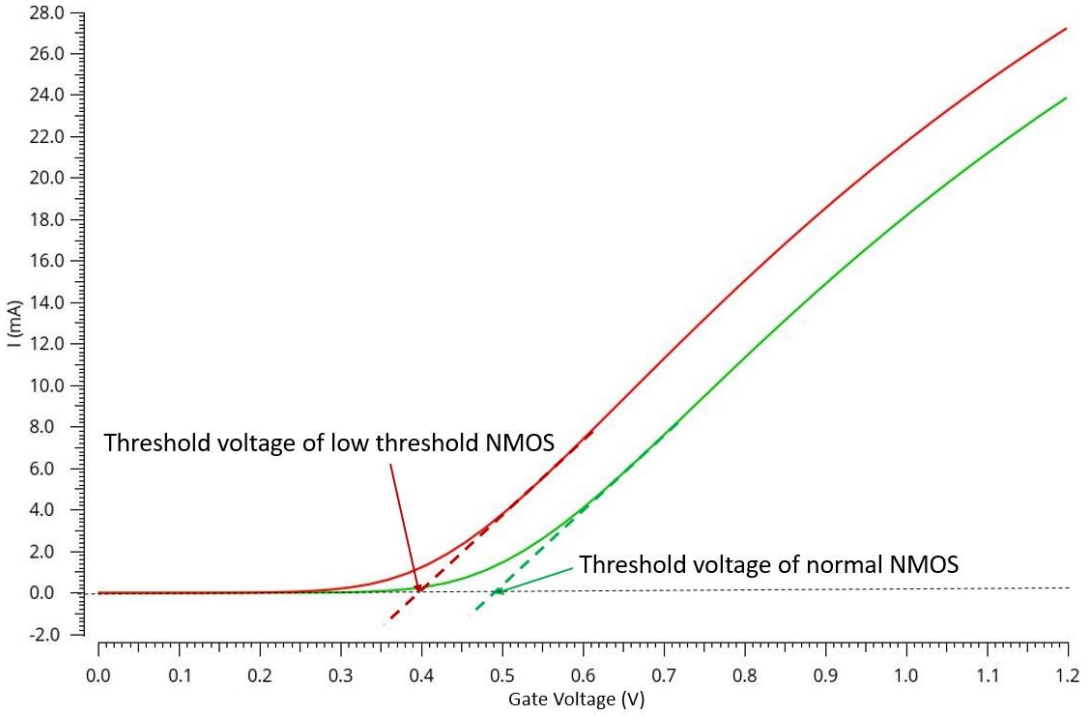

Fig 3.3.2 Threshold voltage measurements of normal NMOS and low threshold NMOS

3.3.2 Varactor

MOS varactor is widely applied on voltage control system as its capacitance can be tuned by gate voltage. In 90 nm process, the offered NMOS type varactor (NCAP) has a bias tuning range from -0.5 V to 1 V. The NCAP device is built with "NFET in n-well" structure as shown in Fig 3.3.3. It is formed by thin gate-oxide over n-well, and N+ implants planted at both sides of n-well to generate resistive contacts in varactor n-well region.

To verify the adjustable capacitance properties of NCAP, a testing band pass filter circuit is built and simulated as demonstrated in Fig 3.3.4. The center frequency of this filter is decided only by inductor and varactor value. In the simulation setup, the inductance and varactor geometry size are fixed, and only use V_{bais} to control the band pass filter center frequency. Simulation results presented in Fig 3.3.5 express the center

frequency changing under different V_{bias} values. It can be seen that when bias voltage equals to -0.5 V, the filter has the highest center frequency of 5.87 GHz because of the smallest capacitance generated at output node by varactor. When bias voltage change to 1 V, varactor creates the largest capacitance which results in the lowest center frequency of filter.

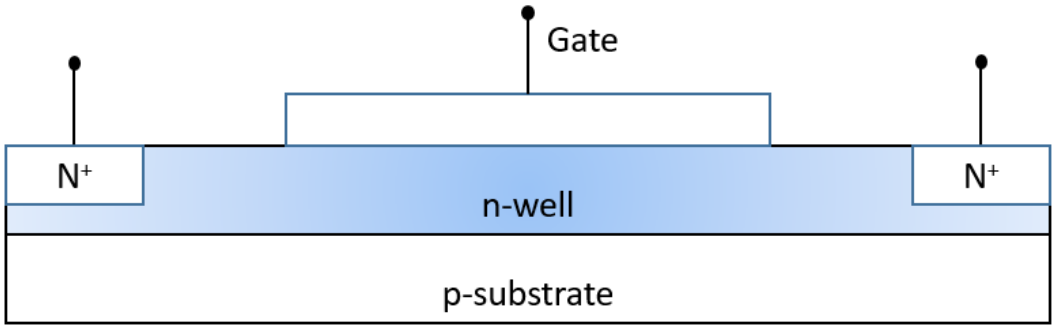

Fig 3.3.3 Cross section diagram of NCAP

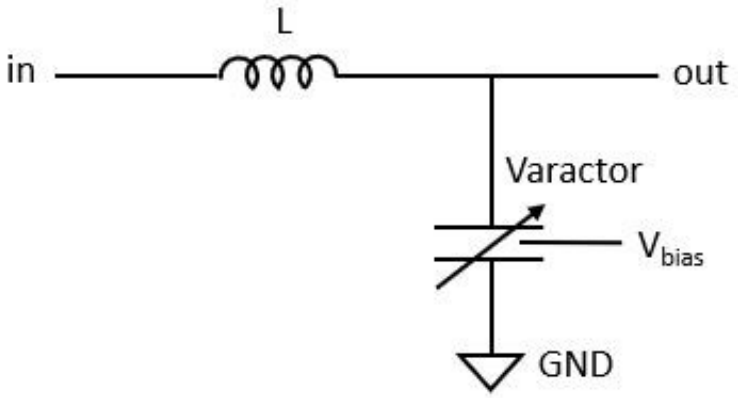

Fig 3.3.4 Schematic diagram of band pass filter built with inductor and varactor

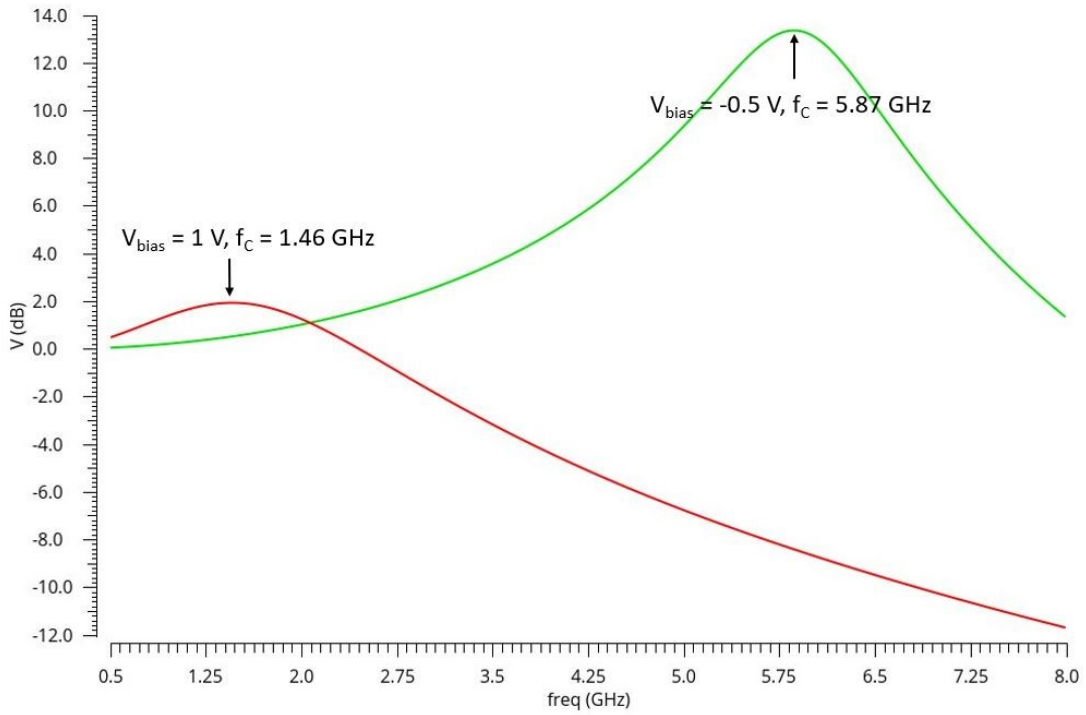

Fig 3.3.5 Center frequency of band pass filter under different gate voltages of varactor

3.4 LNA Implementation and Simulation results

The cascode source de-generation LNA used in this dissertation is built and simulated with 90 nm technology in Cadence software. The circuit schematic is shown in Fig 3.4.1, and the load capacitance (C_{load} + $C_{varactor}$) is set to be 100 fF as previous analysis. Using the theoretical parameter that calculated in previous sections, the LNA employed in this dissertation provides center frequency of 5.25 GHz as shown in Fig 3.4.2. The gain at center frequency is measured as 25.24 dB, and the 3 dB down bandwidth is 717.65 MHz. Since the major task of LNA is suppressing the system noise, the gain and bandwidth shown on simulation result is sufficient to amplify the wanted signal within relatively narrow frequency band and attenuate unwanted signal.

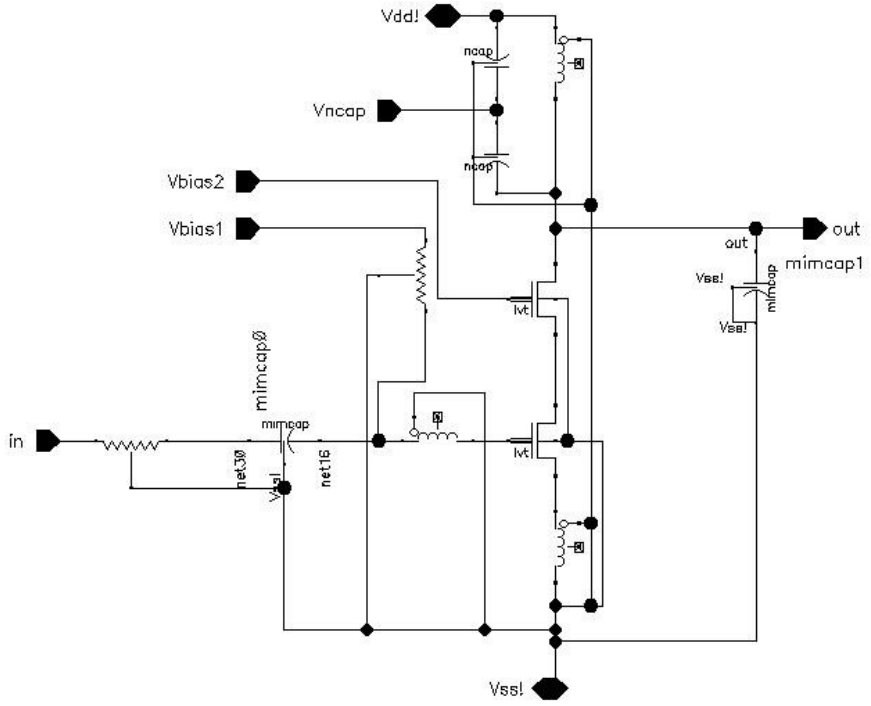

Fig 3.4.1 Schematic diagram of proposed LNA design.

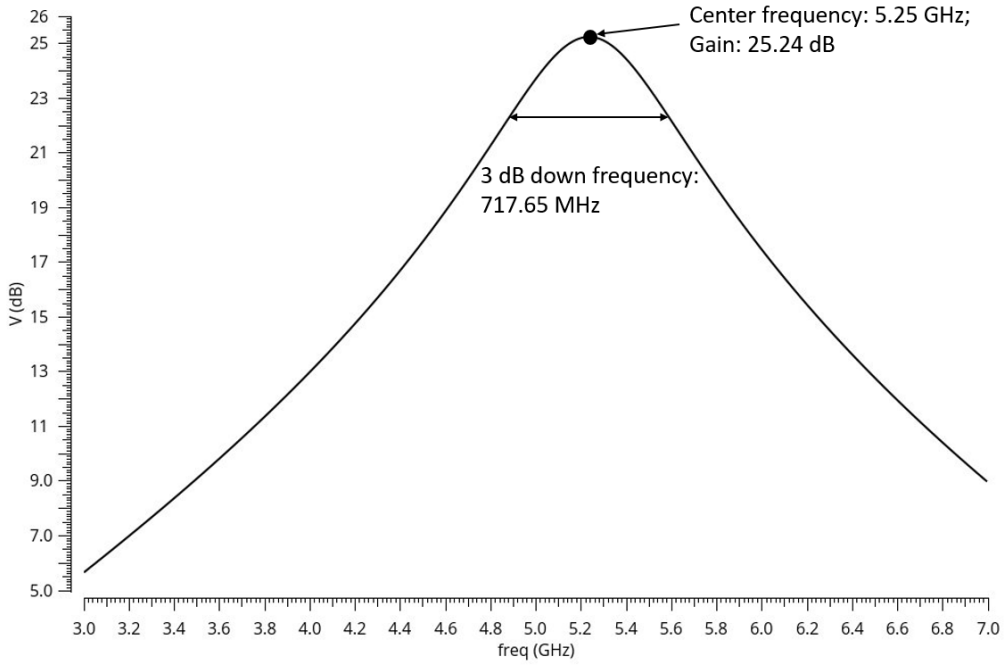

Fig 3.4.2 Simulation results of center frequency, gain, and 3 dB down bandwidth

Quality factor (Q) is calculated as:

$$Q = \frac{f_C}{f_{-3dB}} \tag{3.4.1}$$

Where f_C is the center frequency and f_{-3dB} is 3 dB down bandwidth of simulated circuit. Substitute the simulation result into Eq 3.4.1, the Q of designed LNA is 7.32. This low Q value of implemented circuit is coming from the passive inductor poor quality factor property. As discussed in section 3.1, the passive components have the advantages of low operating noise and non-sensitive to PVT variation, which are the key properties for LNA design. Therefore, to compensate the sacrificed quality factor and gain, an active inductor-based band pass filter is added in the following stages which is demonstrated in next chapter.

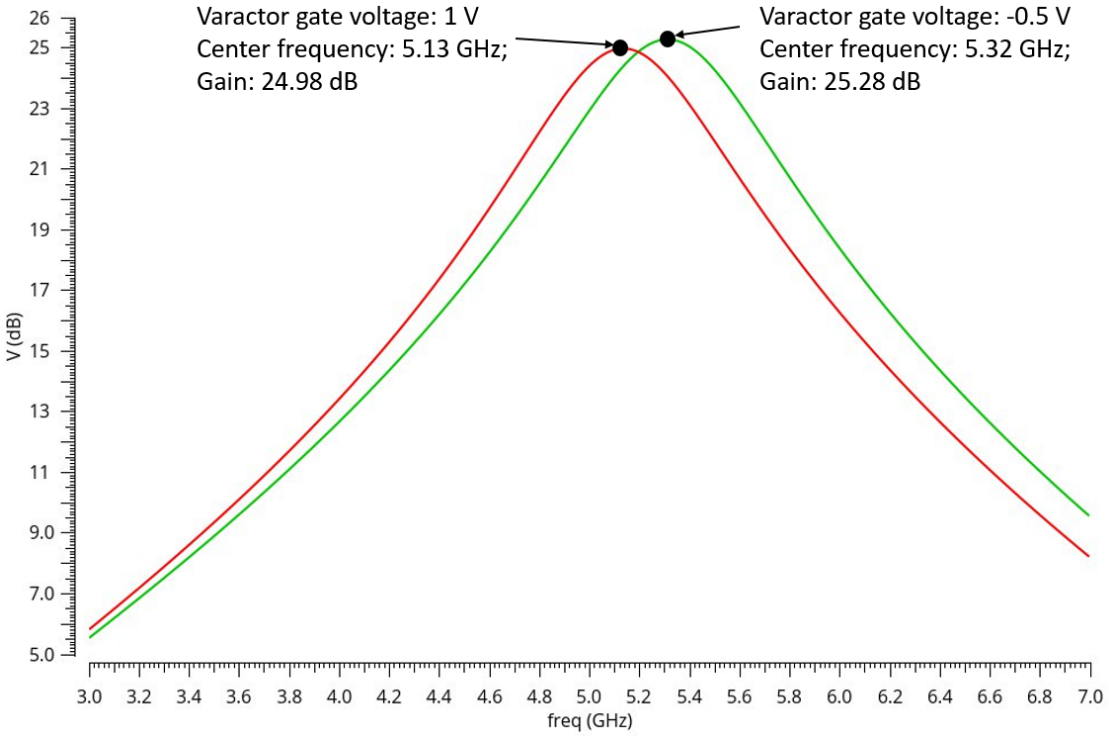

Fig 3.4.3 LNA simulation results of -0.5 V and 1 V varactor gate voltages

Another introduced feature of designed LNA circuit is the capability of adjusting center frequency by connecting a varactor at output node. As shown in previous section, by changing the gate voltage of varactor, the total output capacitance is changed. Thus, the center frequency of LNA can be tuned even after fabrication. In Fig 3.4.3, when gate voltage of varactor set to -0.5 V, the output node capacitance is minimum, and LNA has the highest center frequency of 5.32 GHz. When gate voltage equals to -0.5 V, the maximum output capacitance results in the lowest center frequency of 5.13 GHz. Such frequency difference is large enough for designer to use this LNA on multi-channel application or post-layout compensation.

To evaluate the input impedance matching quality of designed LNA, the Scattering Parameter (S-Parameter) simulation is performed to the circuit. The 2-port S-Parameter is widely used to study the two ports network power waves of reflection and incidence. S_{11} parameter describe the input port voltage reflection coefficient, and smaller value of this number means more power can be delivered to output. Moreover, a good impedance matching circuit is also a pre-filter stage as introduced in section 3.1. Only the signal within selected frequency band is allowed to enter the system and attenuate other noise signal strength including image signal. Fig 3.4.4 contains the S_{11} plot of designed LNA input matching with 50 ohms resistance as requested by system. At 5.25 GHz center frequency point, the measured S_{11} equals to -23.13 dB, and it indicates that a good matching and power transferring performance of this LNA when connected with off-chip 50 ohms resistance.

The Noise Figure (NF) is used to measure the degradation of Signal-to-Noise Ratio (SNR) of designed system. A lower value of this parameter indicates better performance of LNA. In Fig 3.4.5, the designed LNA provides 2.1 dB NF value at center frequency

of 5.25 GHz. Since the gain presented in previous simulation result is 25.24 dB, this number is sufficient to assure a good noise performance of the entire receiver system.

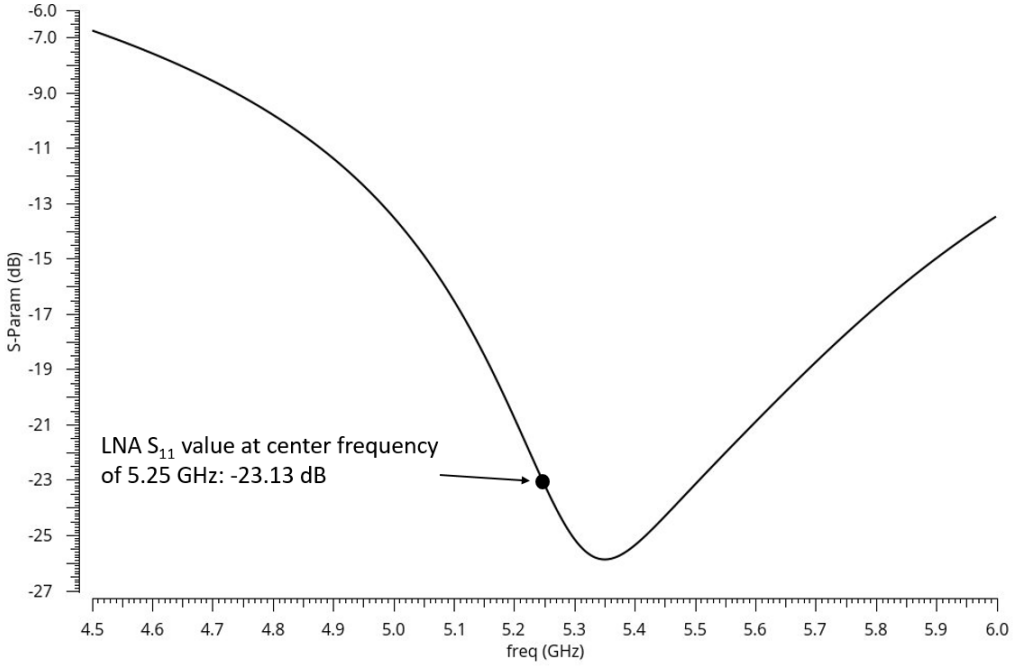

Fig 3.4.4 LNA S_{11} plot.

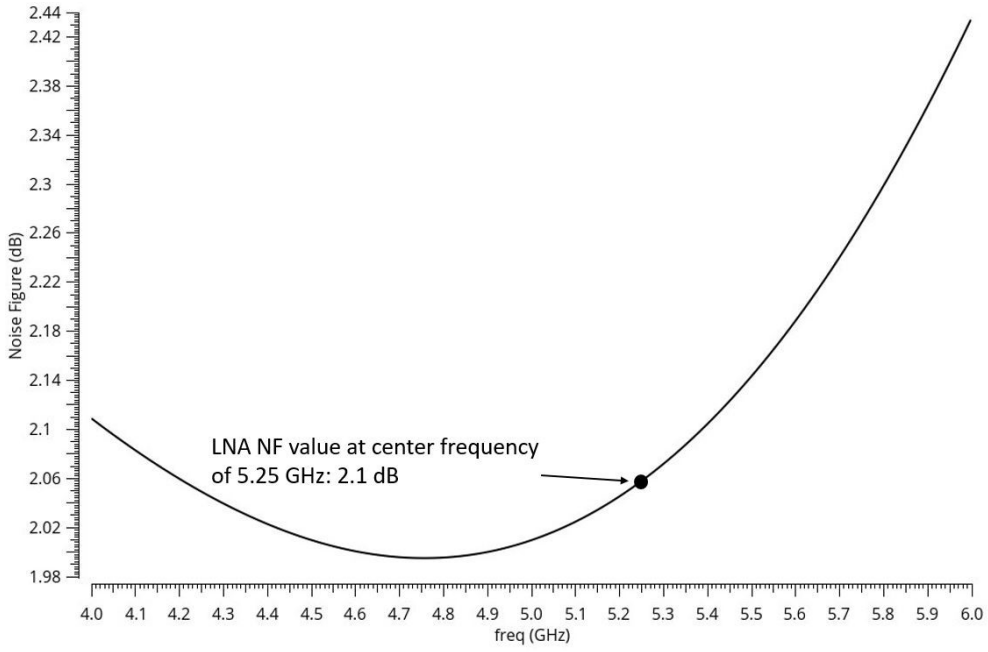

Fig 3.4.5 LNA noise figure plot.

1 dB compression point simulation results are used to evaluate the linearity of testing system. Ideally, for a linear system, the output changing follows the input varying with a constant ratio. However, in practical circuit design, large input signal power causes the saturation of system and the output is no longer linearly following input power increment. Therefore, the point of input power that leads the output dropping 1dB from its expected gain is the 1 dB compression point. Fig 3.4.6 shows the designed LNA has 1 dB compression point of -7.12 dBm at selected channel center frequency of 5.25 GHz.

Another parameter that widely used to describe the system linearity is Input Inferred Third order Intercept Point (IIP3). The third order signals are generated by inputting two fundamental signals into system with frequency close to each other within targeting band. IIP3 value is the point that the fundamental signals and third order signals are all at the same power level. The IIP3 value of proposed LNA circuit is shown in Fig 3.3.11 as -1.54 dBm with the third order signal located at 5.2 GHz.

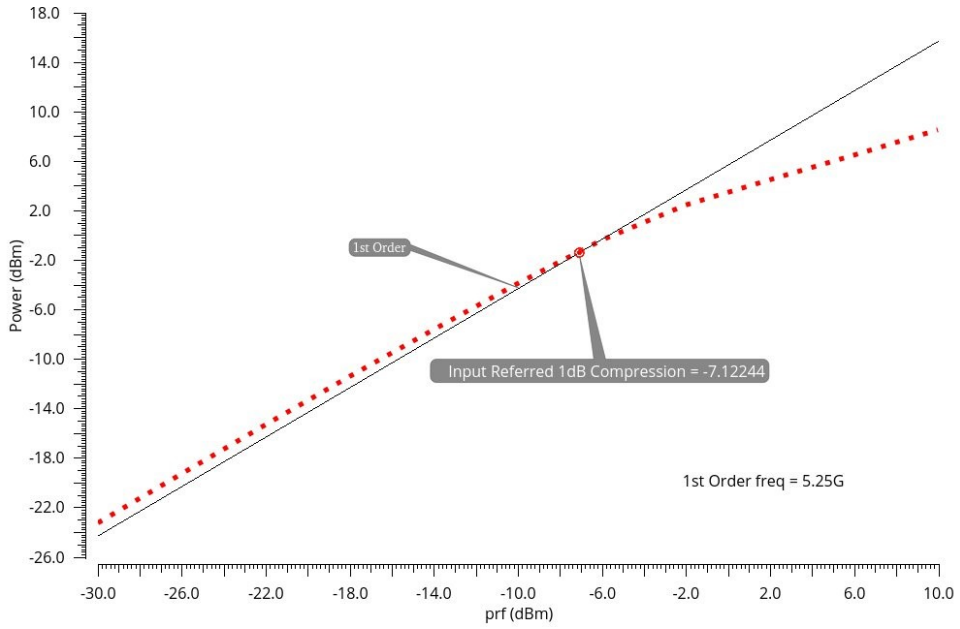

Fig 3.4.6 1 dB compression point simulation result of LNA

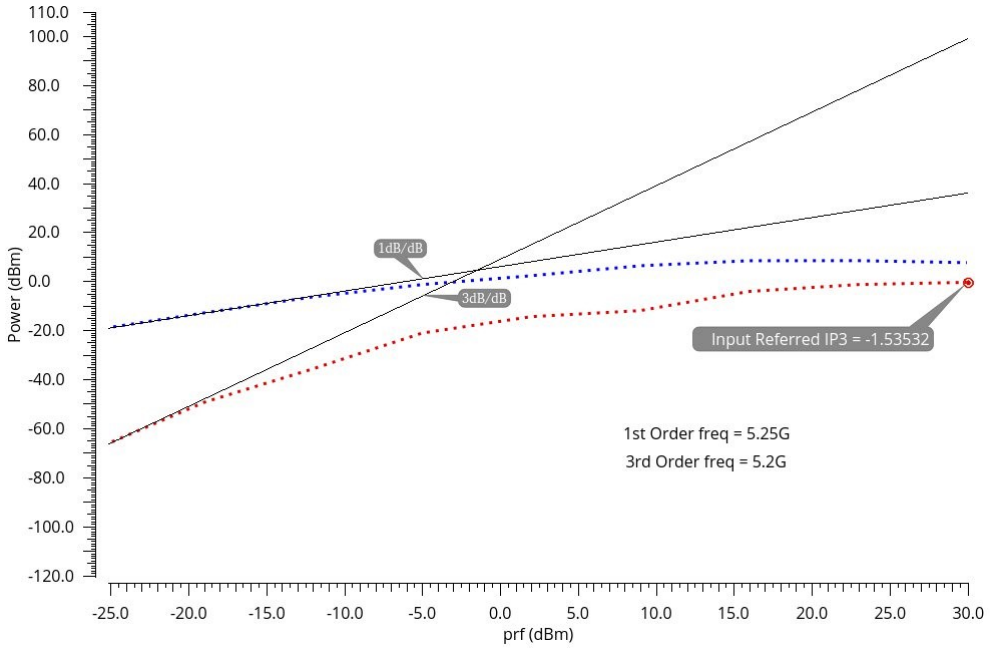

Fig 3.4.7 IIP3 simulation result of LNA

Power consumption of designed LNA is measured as 2.44 mW with input frequency of 5.25GHz and amplitude of 1 mV.

3.5 Conclusion

In this chapter, a cascode source de-generation low noise amplifier is designed and simulated with 90 nm technology. As the first circuit block of receiver system, this LNA has a good input matching property with –23.13 dB S_{11} results at designed center frequency of 5.25 GHz. The 3 dB down bandwidth is 717.65 MHz, so all wanted signal within channel 50 (160 MHz channel bandwidth) of 5 GHz WLAN technology is reserved and amplified by LNA, and out of band noise is attenuated and filtered out. The gain and noise figure of designed LNA is 25.24 dB and 2.1 dB at center frequency, respectively. Such simulation results lay a good foundation of entire front end receiver noise performance. The power consumption of this stage circuit is 2.44 mW with input frequency of 5.25 GHz and amplitude of 1 mV.

IV. Active Inductor Band Pass Filter

(The discussion in the following chapter is substantially drawn from [29]**, where we first reported the development and evaluation of this technique.)**

4.1 Introduction

As discussed in previous chapter, to maintain the LNA stage insensitive to process variation, passive inductors are employed with varactor to implement the first stage circuit of receiver system. The tradeoff of this design is large inductor area and the poor quality factor of the output band pass filter which must be improved by other circuitry in the receiver. The solution provided in this dissertation is placing an Active Inductor-based Band Pass Filter (AIBPF) right after LNA stage to improve the signal quality and system performance. In conventional design, the passive band pass filter is one of the most common circuit block in electric circuit design as it has many advantages like low power consumption, low noise, strong tolerance of large current [30], and high operating frequency. However, for on-chip integrated circuit implementation, the passive inductor-based band pass filter has some critical weakness, such as passive inductor filter lacking wide range tunability [31] and complicated high order filter design being very time-consuming and difficult. The largest drawback is the extremely large on-chip passive inductor size. Thus, active CMOS inductor becomes more and more attractive in recent years. An active inductor only takes 1-10% the area of a passive inductor with same inductance [32]. The AIBPF offers a wider frequency tuning range by adjusting the bias voltage in the circuit. With only one stage design, the AIBPF can provide higher gain and quality factor (Q) than traditional passive design, and potentially can reach even higher value with multiple AIBPFs in cascaded. The adjustable gain feature of AIBPF is also good for on-chip circuit design, as the active filter can be easily converted into VGA with little modification [15].

4.2 Area Consumption of Passive Filters

The conventional band pass filter schematic and frequency response graph is presented in Fig 4.2.1, and the transfer function of this 2nd order filter can be developed below with Ohm's law, and Kirchoff's circuit laws [33].

$$\frac{v_{in}}{R+\frac{sL*\frac{1}{sC}}{sL+\frac{1}{sC}}} * \frac{sL*\frac{1}{sC}}{sL+\frac{1}{sC}} = v_{out} \tag{4.2.1}$$

$$H(s) = \frac{v_{out}}{v_{in}} = \frac{sL*\frac{1}{sC}}{\left(sL+\frac{1}{sC}\right)R+sL*\frac{1}{sC}} \tag{4.2.2}$$

Eq 4.2.2 can be further simplified to

$$H(s) = \frac{sL}{s^2RLC+sL+R} \tag{4.2.3}$$

According to Eq 4.2.3, the order of *s* increases when number of inductive and capacitive components in circuit getting larger. So, for band pass filter design, the general function is

$$H(s) = \frac{a_m s^m+a_{m-1}s^{m-1}+a_{m-2}s^{m-2}+\cdots a_1 s+a_0}{b_n s^n+b_{n-1}s^{n-1}+b_{n-2}s^{n-2}+\cdots b_1 s+b_0} \tag{4.2.4}$$

Eq 4.2.4 indicates that higher order design can give designer more space to optimize the filters performance.

However, the tradeoff of building high order band pass filter is dramatically increasing design complexity and area consumption. For System on Chip (SoC) application, with the technology process scaling down, the unit area cost increasing rapidly. Passive components especially inductor, take huge on-chip design area comparing with active components like transistor. In recent years, this issue draws more attention as the latest wireless systems with most advanced technology are pursuing better performance with smaller size.

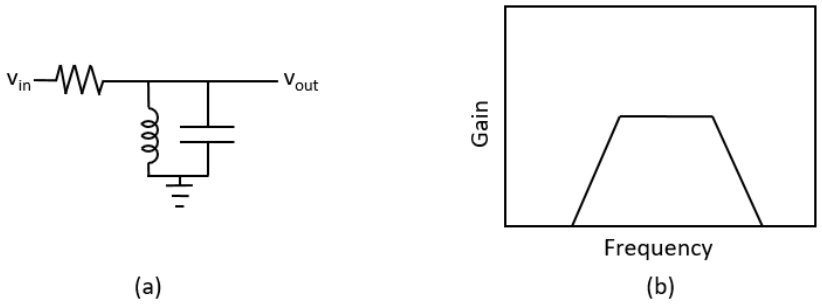

Fig 4.2.1 Schematic and frequency response figure of conventional band pass filter: (a) Schematic (b) Bode plot

4.3 Active Inductor-based Band Pass Filter Operating Theory

To replace the passive inductor in on-chip IC circuits, many design architectures are proposed, and Gyrator-C network is one of the most popular active circuits of emulating passive inductor properties. It is first proposed by Bernard D. H. Tellegen in 1948 [34]. It describes a two-port device containing two transconductors and one output capacitor to achieve the inductor function as shown in Fig 4.3.1 [35]. The equivalent inductance of the gyrator-C network is expressed as Eq 4.3.1 [35] [36].

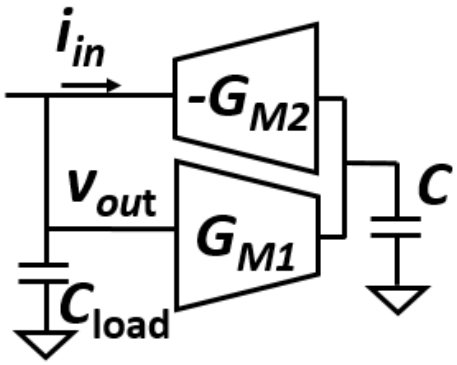

Fig 4.3.1 Gyrator-C network

$$L_{eq} = \frac{C}{(G_{M1} * G_{M2})} \tag{4.3.1}$$

The implementation of the active inductor based on the gyrator/capacitor combination of Fig 4.3.1 is shown in Fig 4.3.2, where M1 is associated with transconductance G_{M1} and M2 to transconductance G_{M2}. M3, M4, and M5 with bias inputs together with *IB* control the quiescent values of G_{M1}, G_{M2}, and G_{M3}. The detailed small signal analysis for this active inductor is developed in [15] resulting in

$$Z_{in} = R_L + sL \tag{4.3.2}$$

In Eq 4.3.2,

$$L = \frac{C}{BG_{M1}G_{M2}}$$

$$R_L \approx \frac{G - Bg_{d3}}{BG_{M1}G_{M2}}$$

$$B \approx \frac{G_{M3}}{g_{d3} + g_{d4}}$$

$$G \approx G_{M2} + G_{M3}$$

And g_{d3}, g_{d4} are the drain conductance of M3 and M4. The result is a value of L controllable by G_{M1}, G_{M2}, G_{M3}, and C together with a small series resistor (R_L) controllable by G_{M1}, G_{M2}, G_{M3}. It is noted that M3 provides another degree of freedom (G_{M3}) together with G_{M1} and G_{M2} to control the value of *L* and *Q* of the active inductor.

The AIBPF using in this dissertation is formed by adding an input transistor producing transconductance G_{M0} and channel resistance r_{ds0} into Fig 4.3.3 to control voltage gain. The small signal equivalent circuit for the AIBPF including a load capacitor C_{Load} is shown in Fig 4.3.4.

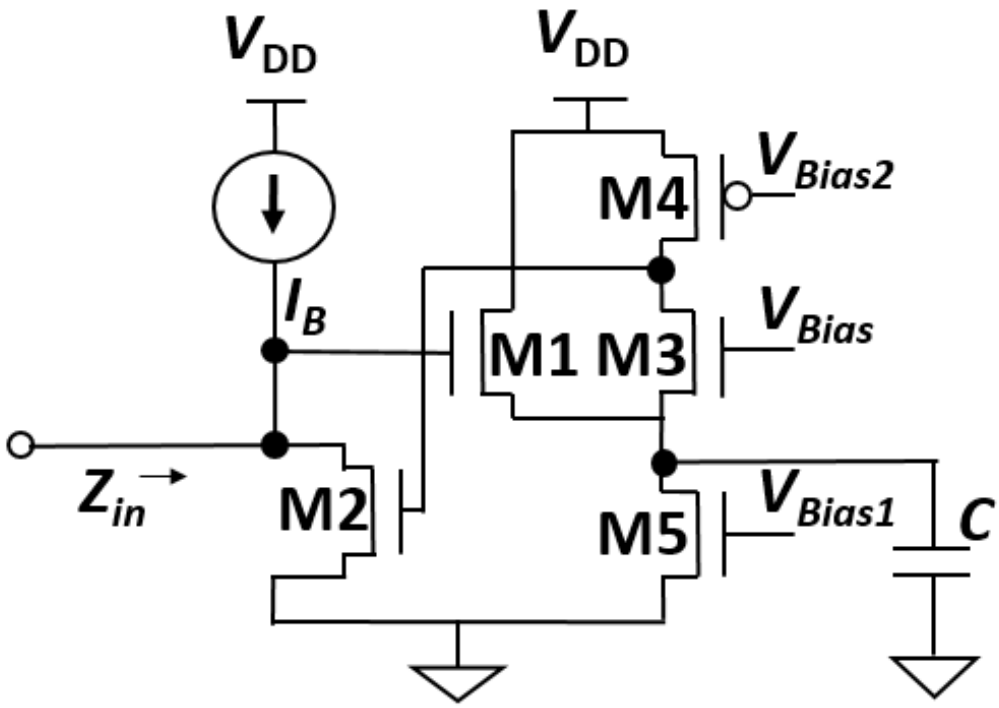

Fig 4.3.2 Schematic of active inductor

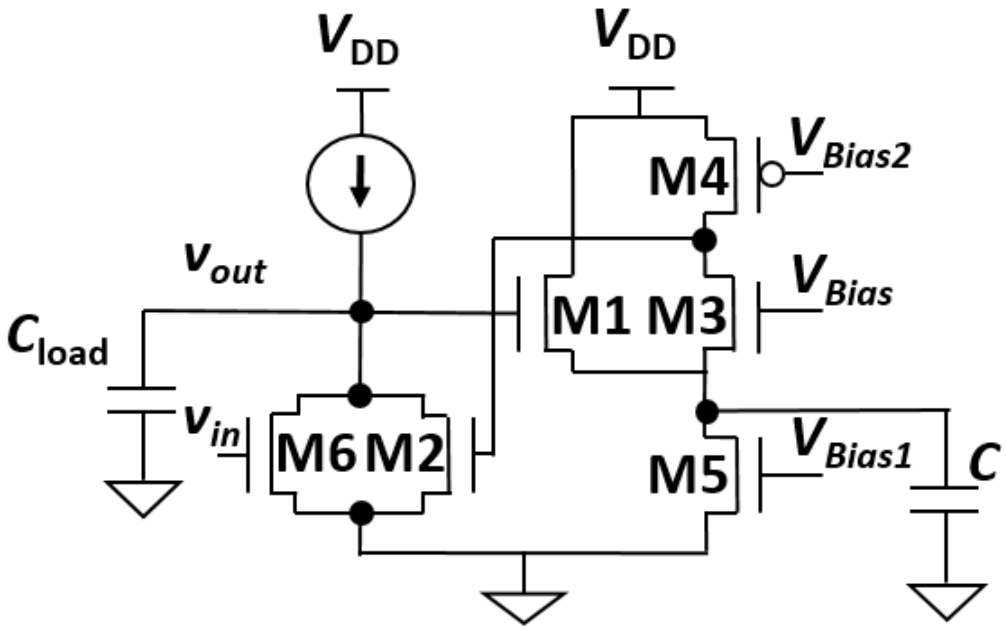

Fig 4.3.3 Schematic of active inductor-based band pass filter

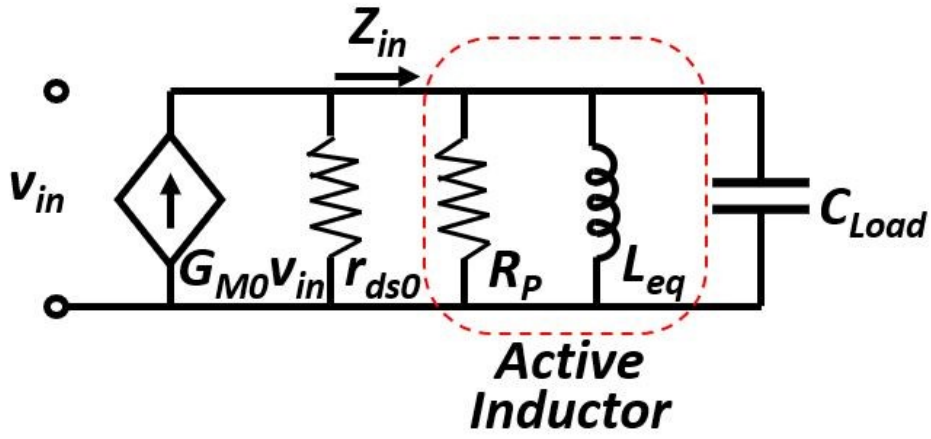

Fig 4.3.4 Small signal model of AIBPF

In Fig 4.3.4, L_{eq} and R_P are the inductance and parallel loss resistance of active inductor respectively. And

$$R_P = \frac{(\omega_0 L_{eq})^2}{R_L} \tag{4.3.3}$$

$$R_{eff} = \frac{R_P}{\omega_0 L_{eq}} \tag{4.3.4}$$

So, the center frequency (f_C) of this G_m-C network band pass filter is

$$f_C = \frac{1}{2\pi\sqrt{L_{eq}C_{load}}} = \sqrt{\frac{G_{M1}G_{M2}G_{M3}}{4\pi^2(g_{d3}g_{d4}C_{load}C)}} \tag{4.3.5}$$

The quality factor of AIBPF is:

$$Q = \frac{R_{eff}}{\omega_0 L_{eq}} \tag{4.3.6}$$

$$A_v = G_{M0}R_{eff} \tag{4.3.7}$$

As seen in Eq 4.3.5, the center frequency is tunable by varying G_{M1} and G_{M2}, and G_{M3} with the transconductance is proportional to the quiescent bias current and transistor gate voltage; so, post fabrication center frequency tune-ability is possible with either external or on-chip bias control.

4.4 Simulation Result

In this dissertation, all the circuit constructions and simulations are performed by Cadence using 90 nm technology. There are two methods used to analyze the process variation: corner analysis and Monte Carlo analysis. Corner analysis is simulating the different running speed of circuits assuming all transistors are fabricated at corner process conditions. For both PMOS and NMOS transistors, each of them has three corners and they are: Slow (S), Typical (T), and Fast (F). Such corners usually indicate the transistor speed changing based on PVT effect. For example, the slow corner reflects the impact of low operating voltage and high environment temperature. The corner analysis is used to estimate the circuit performance under extreme PVT variation. Thus, the corner analysis is always used as coarse evaluation of system PVT tolerance.

Monte Carlo analysis assumes a statistical variation of process parameters and component mismatch. It uses more complicate mathematic model to simulate the PVT variation and lets designer do detailed analysis of circuit performance under different variation. This method is good for the design that has already passed the corner analysis and need to be further tested with simulation condition closer to reality.

Fig 4.4.1 presents the schematic diagram of proposed AIBPF, and the frequency response plot of this circuit is shown in Fig 4.4.2 with center frequency adjusted to 5.25 GHz. The gain of this system at center frequency is 28.8 dB and 3 dB down frequency bandwidth is 140 MHz.

However, the sensitivity to transconductance change also makes the AIBPF vulnerable to process variations and component mismatch during fabrication. Fig 4.4.3 shows the frequency response of AIBPF with the same design parameter but different process corner. AIBPF produces a lower center frequency under slow-slow corner and higher value under fast-fast corner.

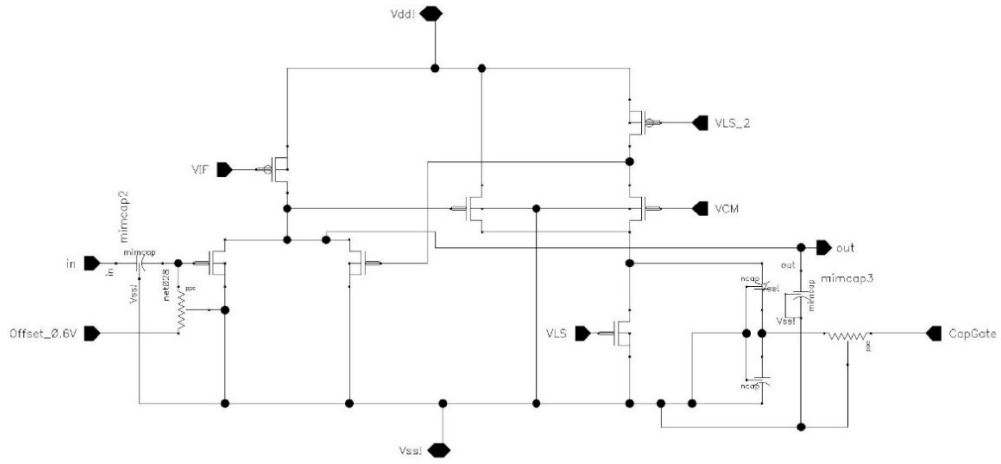

Fig 4.4.1 Schematic diagram of proposed AIBPF.

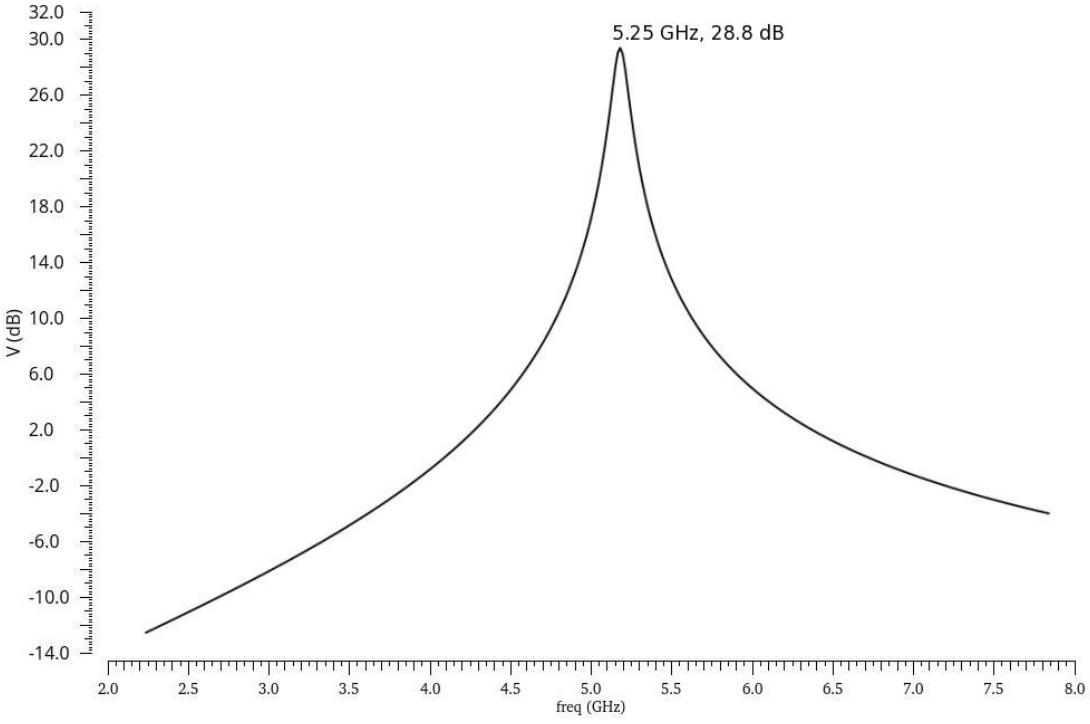

Fig 4.4.2 Frequency response plot of AIBPF

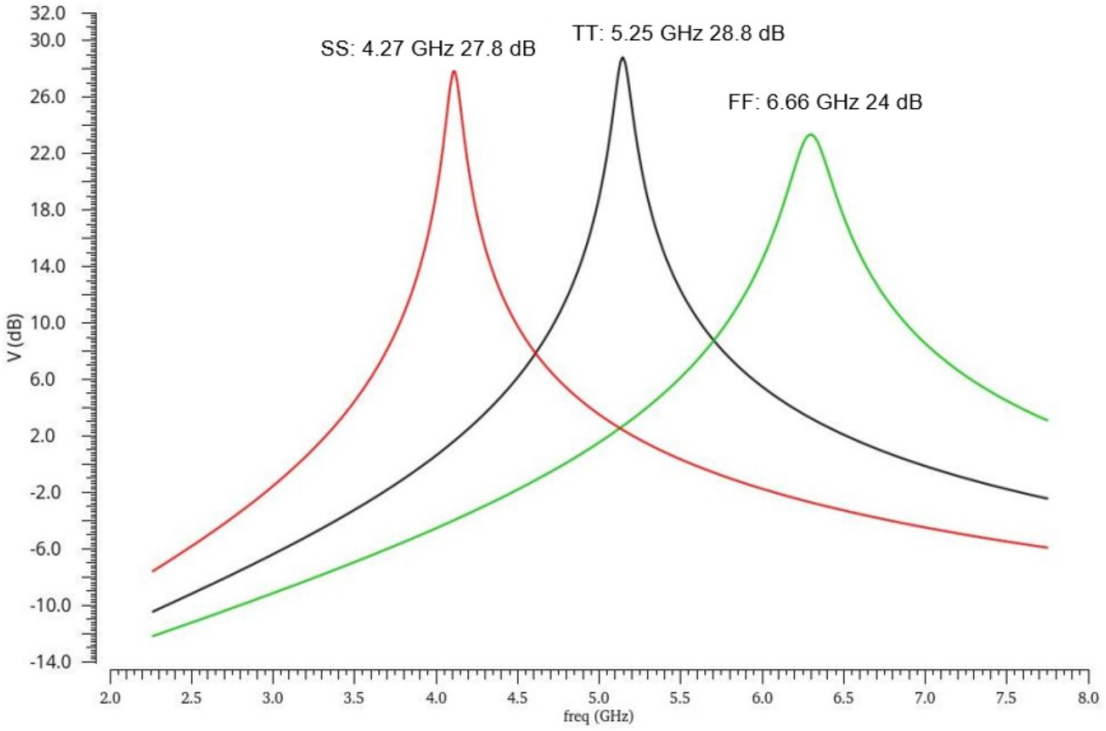

Fig 4.4.3 AIBPF frequency response under different process corner

Moreover, as demonstrated in Fig 4.4.4, the possibility of center frequency shifting out of 3 dB down bandwidth caused by process variation is typically more than 70% based on simulation results in 90 nm CMOS technology when AIBPF is built for high frequency applications. This sensitivity of the AIBPF performance to process variation in Fig 4.4.4 is based on the results of 50 Monte Carlo simulations. The Monte Carlo results show that only 8 of the 50 Monte Carlo results (16%) have the center frequency within the desired 3 dB bandwidth. This corresponds to 84% of the post fabrications filters needing calibration to reset the center frequency within the desired 3 dB bandwidth.

To overcome the process variation issue of active circuit, an automatic on-chip post-fab calibration system is needed to correct center frequency changes and increase the yield of integrated circuits incorporating AIBPFs. The calibration system should be able to capture the center frequency error, analyze variation type, and compensate

process variation automatically. In next 2 chapters, two key components: amplitude detector and analog buffer are introduced to be part of the self-calibration system. The CMOS amplitude detector is used to realize the error acquisition function. The analog buffer is placed inside the system to help increase the driving ability of on-chip circuit and isolate adjacent circuit blocks. The completed AIBPF self-calibration system is demonstrated in chapter 7 including the design mechanism and simulation result.

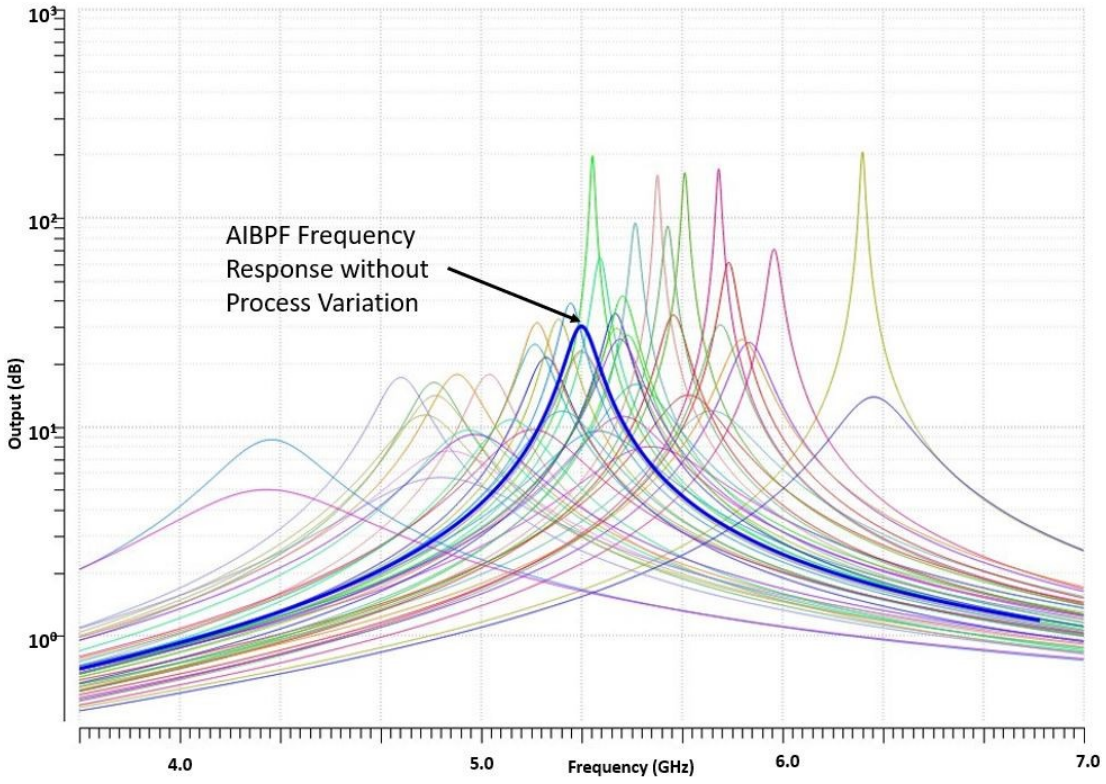

Fig 4.4.4 Process variation effect on AIBPF (simulated with Monte Carlo Analysis)

V. CMOS Amplitude Peak Detector

(The discussion in the following chapter is substantially drawn from [37]**, where we first reported the development and evaluation of this technique.)**

5.1 Introduction

As mentioned in previous chapters, with the rapid development of CMOS process technology, active inductor has been applied in some SoC designs especially for band pass filter application to save area [15]. Nevertheless, the fatal drawback of this solution is process variation which results in center frequency and gain changing. To fix such variation, a built-in self-testing (BIST) circuit can be employed as part of calibration circuit block [38]. A wide output range CMOS amplitude peak detector becomes an important integral part of calibration stage to realize the real-time monitoring function.

In this dissertation, a unique simple peak detector reported in [39] is used and modified with detailed theoretical analysis of circuit operating properties.

5.2 Theoretical Analysis

5.2.1 Two-State Amplitude Peak Detector Implementation

The schematic diagram of the proposed CMOS peak detector is depicted in Fig 3.2.1, which consists of two stages. First stage is referred from [39] to detect input amplitude and convert it into DC value.

As shown in Fig 5.2.1, I_{bias} is the current source generated by transistor $M2$. I_1 is the current flowing through $R_{feedback}$, essentially $M1$ transistor gate leakage current, which is very small. Thus, the voltage drop across $R_{feedback}$ is quite small. First stage output, V_1 DC voltage, feedbacks to $M1$ gate to provide the DC gate voltage. When input amplitude increases, to have $M1$ current I_{M1} balanced with I_{bias}, the gate/drain voltage of $M1$ must be reduced to adjust the current. Therefore, the drain voltage of $M1$

(V_1) can successfully express the input amplitude changing, and V_1 DC voltage increment is inversely proportional to v_{in} signal amplitude growing. Such detection result is held by capacitor C_2 as DC voltage with coupling jitter. $M1$ transistor size is large to have V_1 changing widely following input amplitude change.

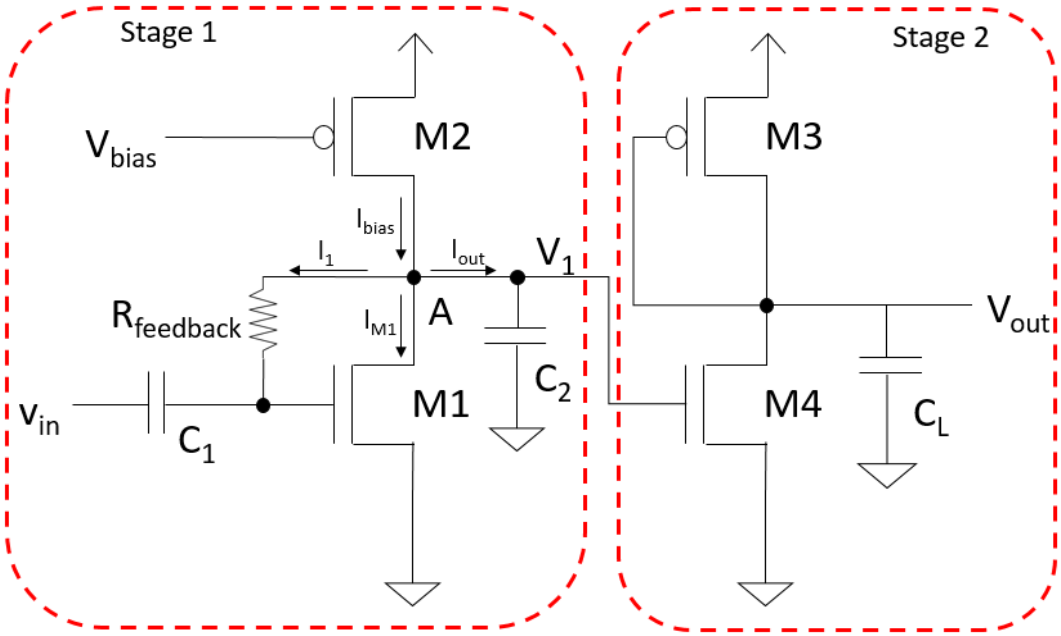

Fig 5.2.1 Schematic of proposed CMOS peak detector.

However, V_1 is also the DC voltage for $M1$ gate, and theoretically the value of V_1 must be greater than threshold voltage of $M1$ to keep $M1$ on. To satisfy such voltage limitation, the first stage output V_1 varying range becomes smaller. Refer to the data of [39], by using only first stage circuit, the output DC voltage range is 400 mV to 50 mV corresponding to input amplitude of 100 mV to 500 mV with 180 nm process of 1.8 V supply voltage. It appears $M1$ is operating in cutoff region for some cases unless the blocking capacitor $C1$ is small and the input DC voltage couples to $M1$ gate directly. From the data, it can also be seen that the detection output reflects the input amplitude inversely, and the ratio between maximum input peak to peak value and supply voltage is 0.56, which is not suitable for designs require large bias voltage adjustment range.

The objective of this paper is to enlarge the peak detector output range and have the output reflects the input signal amplitude directly.

To flip the detection results generated from first stage, an active load amplifier (*M*3 and *M*4 transistors), is added as second stage circuit shown in Fig 5.2.1. The output of second stage is inverted, and can be expressed as Eq 5.2.1

$$v_{out} = -g_{m4}v_1 * r_{out2} \tag{5.2.1}$$

Where,

$$r_{out2} = \frac{1}{(g_{m3}+g_{ds3}+g_{ds4})} \approx \frac{1}{g_{m3}} \tag{5.2.2}$$

Since g_{ds3} and g_{ds4} are much smaller than g_{m3}, r_{out2} is inversely proportional to g_{m3}. In order to have large r_{out2} at v_{out} node, *M*3 must have a small width, as the trans-conductance of transistor is proportional to its width [26]. At the same time, enlarging the width of *M*4 transistor can increase the trans-conductance value, g_{m4} in Eq 5.2.1. With the transistors width setup based on above analysis, the second stage active load amplifier enhances the detection result range, also inverts the DC output trend from inversely proportional to input amplitude change at v_1 to proportional to the growth of input amplitude at v_{out}.

5.2.2 Output Coupling Jitter Analysis

Output coupling jitter (also called AC gain) is very important for peak detector design. As the expected detection result is a DC voltage, and the jitter coupled on output must be as small as possible. Ideally, the jitter gain of first stage circuit is zero, so that the output signal of peak detector is a perfect DC signal, and next stage circuit result can be more accurate. To analyze jitter performance of this peak detector, a small signal equivalent circuit is employed in Fig 5.2.2 by assuming *C*2 (1 pF) is much larger than gate capacitance of *M*4 and parasitic capacitance of *M*1, *M*2. The goal is to find the

lowest jitter gain with respect to $R_{feedback}$ to reduce the jitter amplitude coupling on output DC signal of first stage.

Referring to Fig 5.2.2 at node A, apply KCL equation:

$$g_{m1}v_{gs1} = i_1 + i_2 \tag{5.2.3}$$

i_2 is the AC current flowing through r_{out1}, which equals to r_{ds1} in parallel with r_{ds2}.

$$v_1 = -i_2 * r_{out} \tag{5.2.4}$$

At the same time, i_1 can be expressed by

$$i_1 = \frac{(v_{in}-v_1)}{R_{feedback}} \tag{5.2.5}$$

Substitute i_1 into Eq 5.2.3

$$i_2 = g_{m1}v_{gs1} - \frac{(v_{in}-v_1)}{R_{feedback}} \tag{5.2.6}$$

Apply Eq 5.2.6 to Eq 5.2.4, then

$$v_1 = \frac{(v_{in}r_{out1}-g_{m1}v_{gs1}r_{out1}R_{feedback})}{(r_{out1}+R_{feedback})} \tag{5.2.7}$$

Since r_{out1} is much larger than $R_{feedback}$, Eq 5.2.7 becomes,

$$v_{in} - g_{m1}v_{gs1}R_{feedback} = v_1 \tag{5.2.8}$$

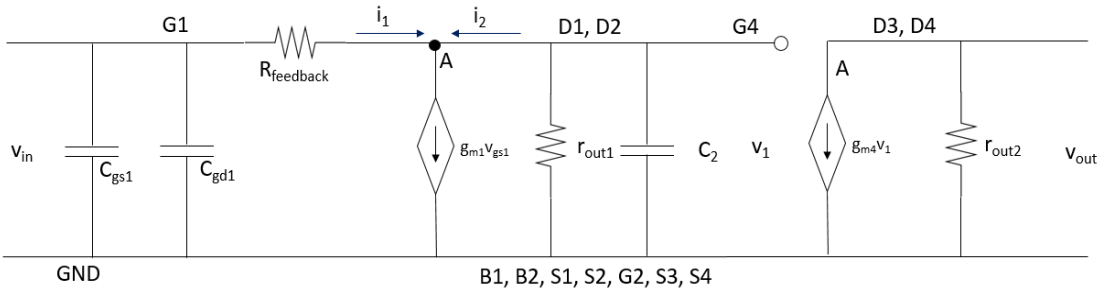

Fig 5.2.2 Small signal equivalent circuit of CMOS peak detector

Where $v_{gs1} = v_{in}$, so that, the jitter gain of first stage is

$$A_{v1} = 1 - g_{m1}R_{feedback} \tag{5.2.9}$$

In order to minimize the jitter amplitude at V_{out} node, the jitter gain of first stage circuit, A_{v1}, must be close to 0. This requires $g_{m1}R_{feedback}$ as close to 1 as possible, according to Eq 3.2.9. Based on first stage simulation results, the maximum value for g_{m1} is 5133.3 μA/V^2, and the minimum value is around 1426.8 μA/V^2 on the basis of transistor width of M1, 18 μm and *M*2, 1.5 μm. Thus, the resistance range of feedback resistor is within 195 Ω and 700 Ω. $R_{feedback}$ is also used to block the AC current flowing between *M*1 gate and drain, so the resistance is required to be as large as possible. Therefore, choose the estimated value of $R_{feedback}$ to be 700 Ω.

The second stage active load amplifier circuit is also designed to have low bandwidth to attenuate the high frequency jitter amplitude based on 3 dB down frequency equation:

$$f_{-3dB} = \frac{1}{2\pi * r_{out} * C_L} \tag{5.2.10}$$

In (10), C_L is load capacitance, and it is fixed by next stage circuit architecture. Therefore, when r_{out2} getting larger, the circuit has smaller 3 dB down frequency. Referring to the analysis results from section 5.2.1, *M*3 transistor size need to be small to have large equivalent resistance. So that, with the reduced *M*3 transistor size, the 3 dB down frequency value of the second stage circuit decreased, and the active load amplifier circuit can further weaken the coupling jitter amplitude at V_{out} node. In conclusion, in order to enlarge the voltage difference between every two adjacent DC detection results and minimize the coupling jitter amplitude on DC output, the *M*3 transistor size should be small to provide large equivalent resistance.

5.3 Layout Simulation Results

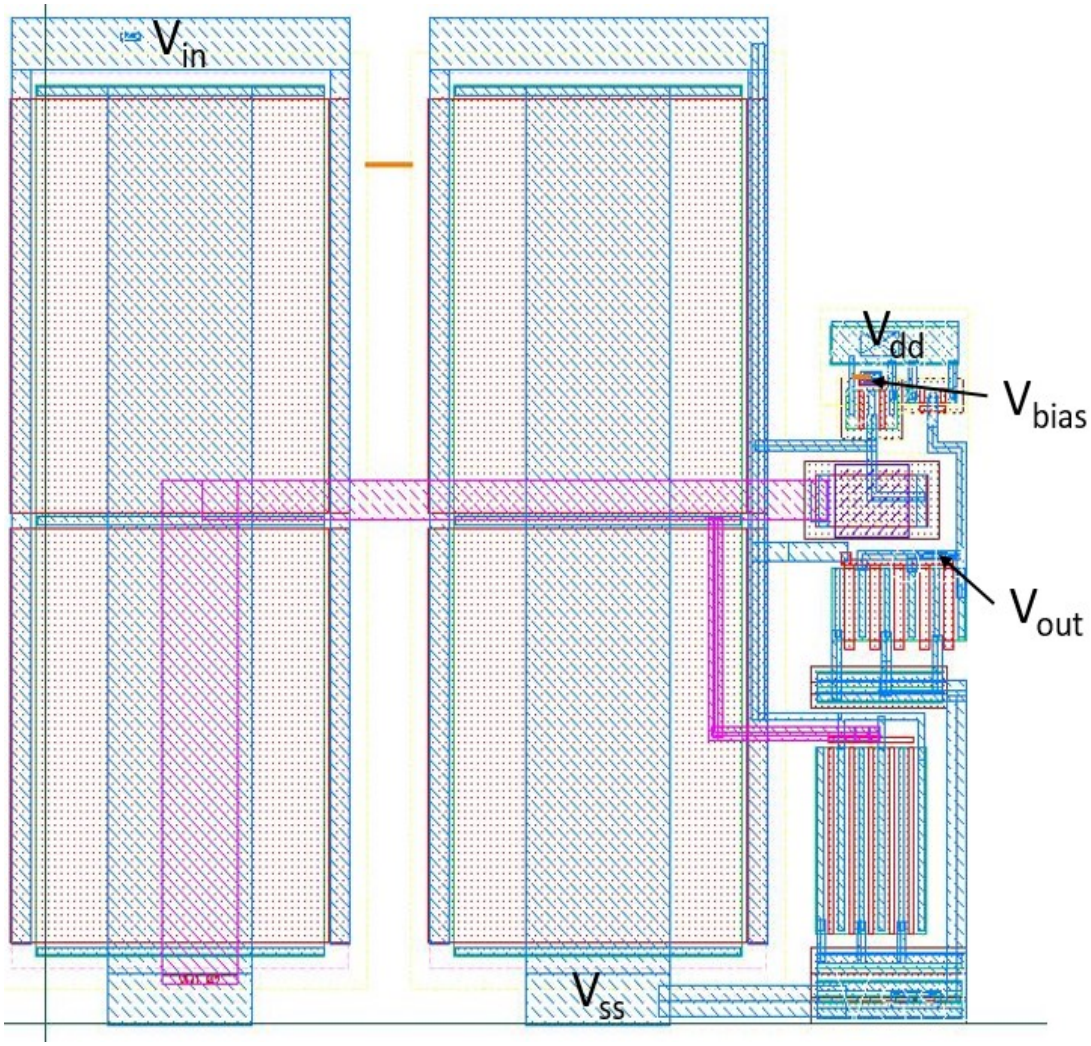

Fig 5.3.1 Layout of proposed CMOS amplitude peak detector using 90 nm technology

Based on section 5.2.1 and 5.2.2 analysis, the proposed CMOS peak detector is implemented in CMOS 90 nm technology with layout shown in Fig 5.3.1. To verify the theoretical analysis of feedback resistor value, the feedback resistance is set to be a variable that sweeping from 195 Ω to 800 Ω. Input signal has 100 mV amplitude and 6.0 GHz frequency. Fig 5.3.2 contains the output jitter results with $R_{feedback}$ of 195 Ω, 580 Ω, and 700 Ω, and it shows the proposed peak detector having the minimum output jitter amplitude when feedback resistance equals to 580 Ω. Fig 5.3.3 summarizes the

jitter amplitude changing with $R_{feedback}$ changing step size of 10 Ω between 195 Ω and 800 Ω. Through the graph, 580 Ω feedback resistor gives the minimum jitter amplitude, 72.35 μV. However, when $R_{feedback}$ is within 550 Ω and 650 Ω range, the jitter amplitude is near the same. Based on output jitter results, in this paper, $R_{feedback}$ is set to be 580 Ω, which matched the analysis conclusion in section 5.2.1 and 5.2.2.

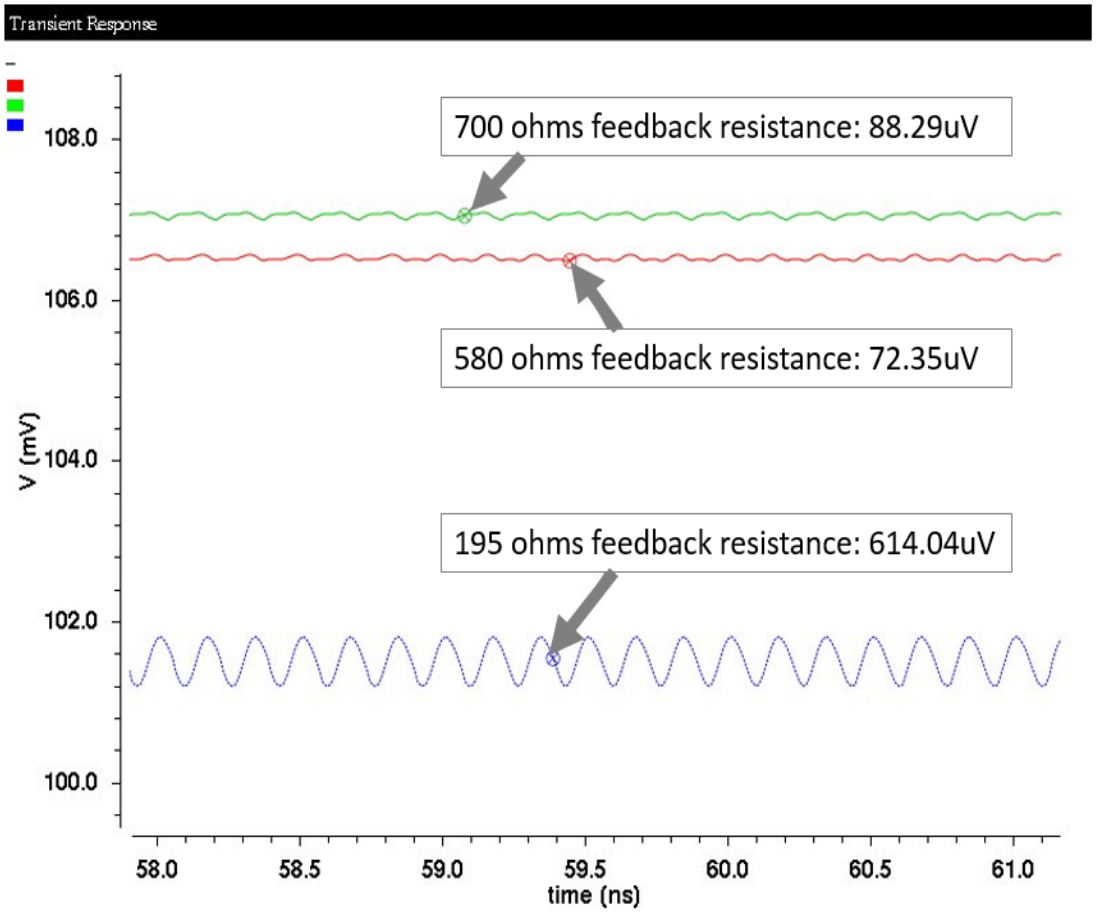

Fig 5.3.2 Jitter results with 195 ohms, 580 ohms, and 700 ohms feedback resistance

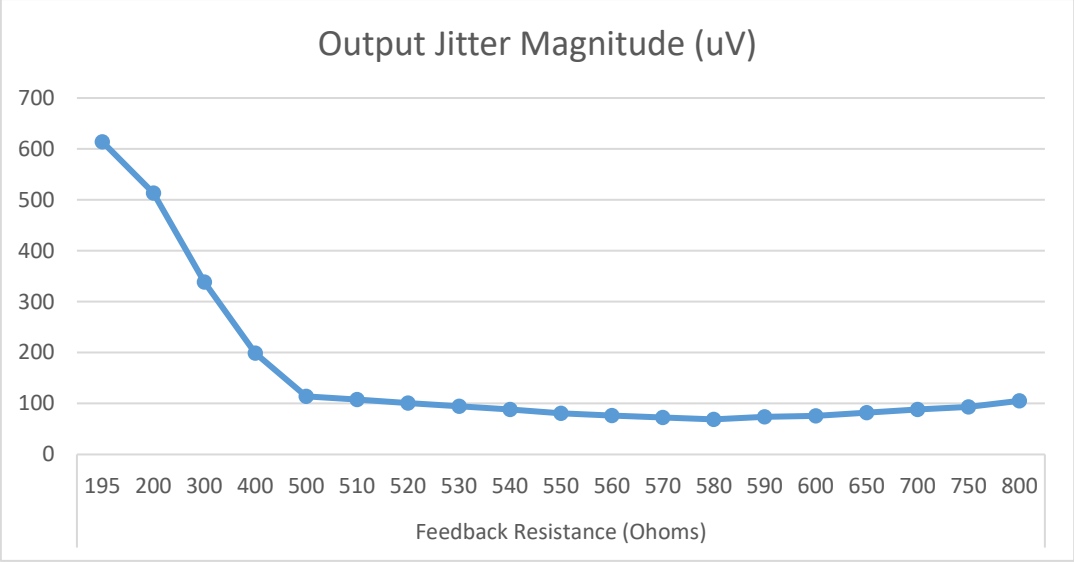

Fig 5.3.3 Output jitter amplitude data plot of feedback resistance sweeping from 195 ohms to 800 ohms with fine simulation between 500 ohms and 600 ohms.

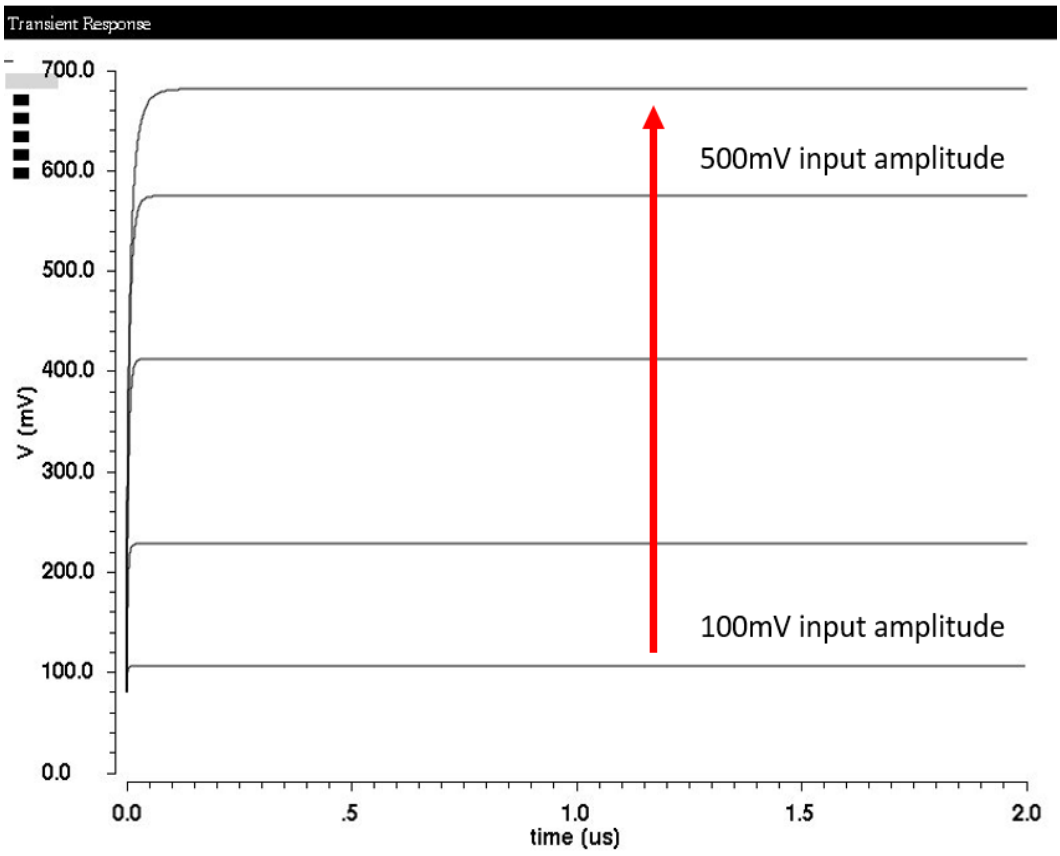

Fig 5.3.4 DC detection simulation result of input amplitude sweeping from 0.1 V to 0.5 V at 6.0 GHz frequency.

Layout simulation results in Fig 5.3.4 show the proposed peak detector can well distinguish different input amplitude with 1.0 pF capacitive load and 6.0 GHz input frequency. As seen in Fig 5.3.4, with 500 mV input amplitude, the peak detector output is 680 mV. The ratio between maximum input peak to peak value and supply voltage is 0.83, and that means the capability of input amplitude acceptance for proposed design is better than the design in [39], whose ratio equals to 0.56. The largest output difference between two adjacent 100 mV input amplitude (200 mV to 300 mV) is about 186 mV, and the smallest is 106 mV while the input amplitude changing from 400 mV to 500 mV. Such large output range makes next stage circuit recognize the active circuit working status easily. If PVT variation happens, the peak detector's output DC value changes to reflect the error. Then, the calibration circuit can be activated by this error, and send compensation signal to eliminate PVT variation.

Table 5.3.1 summarizes the performance comparison of this proposed design with previous reported designs. It can be seen that the proposed design is very competitive compared with other peak detector designs. The operating frequency is the highest and the power consumption is the lowest among all four designs.

Table 5.3.1 Simulation Summary and Comparison

Reference	[40]	[38]	[39]	**Proposed**
CMOS Process (nm)	180	350	180	**90**
Measured Operation Frequency (GHz)	5.2	0.9 - 2.4	2.5	**6.0**
Detection DC Output Range (mV)	-	-	50-400	**100-700**
Driving Ability (pF)	-	0.6	-	**1**
Supply Voltage (V)	1.8	3.3	1.8	**1.2**
Power Consumption (mW)	3.5	8.6	-	**0.4**

Low power benefits from more advanced technology, and small size of current source transistor in first stage that limits the current. Cadence layout simulation results show this proposed peak detector can detect input amplitude of 100 mV to 500 mV from frequency 1.0 GHz to 10.0 GHz

5.4 Conclusion

The CMOS peak detector introduced in this chapter can be used for on-chip self-calibration application. The proposed peak detector can successfully detect different input amplitude by outputting different DC voltages. The detective input frequency range is 1.0 GHz to 10.0 GHz with 1 pF capacitive load. The power consumption is 0.4 mW with input amplitude of 500 mV and frequency of 6.0 GHz and power supply of 1.2 V. The low power cost, high input frequency range and wide output voltage range make this proposed CMOS peak detector is suitable for most on-chip applications.

VI. Analog Buffer

(The discussion in the following chapter is substantially drawn from [41], where we first reported the development and evaluation of this technique.)

6.1 Introduction

The unity gain analog buffer is a key component for RF mixed signal integrated circuit design. The task of the unity gain analog buffer is to drive a relatively large on chip capacitive load (C_L) over a wide frequency range with near unity gain while presenting a small input capacitance (C_{in}) to the previous stage. Also, the buffer must be able to isolate two stages circuit and prevent the interference from one to another.

For high frequency operation, one objective is to maximize the 3dB bandwidth for a specified ratio C_L/C_{in}. The required value of C_{in} and the ratio of C_L/C_{in} varies depending on the application and the technology. For example, a 90 nm CMOS application may typically require the on-chip buffer to present a C_{in} value of approximately 10 fF while driving load capacitance in the range of 50 fF to 250 fF. It should be noted that the effective output load C_{out} includes the load capacitance C_L and the self-loading capacitance on the output node of the buffer (C_{SL}). Linearity is another important requirement for an on chip buffer since it must be capable of operating with a relatively large dynamic range of input/output amplitudes. Measures of performance include maximum input amplitude, variation of gain over the range of input amplitudes (gain accuracy), total harmonic distortion (THD), low frequency gain, and offset error (input offset-output offset). Maximum input amplitude is determined in this analog buffer design based on a range of input magnitudes where the variation in gain is less than 2%. The tolerance for gain variation varies for a particular application, so maximum input amplitude may vary accordingly.

6.1.1 Source Follower Based Unity Gain Buffers

The source follower has been the classical circuit for implementing a unity gain buffer [27]. Since the source is the output node, the device threshold varies due to the body effect as the input increases resulting in relatively poor linearity. The body effect can be alleviated by cascading NMOS and PMOS source follower circuits and/or connecting the source to bulk in an isolated well; however, gain accuracy (linearity), offset, and loss of gain are usually not sufficient for many applications. Several modifications have been made to the basic source follower circuit to reduce offset and increase linearity. Negative feedback has been introduced in various ways to increase gain accuracy [42] [43] [44]. These designs, which include a combination of a feedback amplifier and source follower improve gain accuracy but suffer from reduced input/output amplitude range (maximum input amplitude) for advanced technologies with reduced value of V_{dd}. Also, the introduction of a high gain amplifier requires assessment of stability with the addition of a compensation capacitor in most cases and a corresponding reduction in 3 dB bandwidth. Another performance issue associated with the source follower buffer is the tradeoff between source follower transistor size and 3dB bandwidth. The output resistance of the source follower is proportional to $1/(g_{mSF}+g_{mCurrent\text{-}source})$, where, g_{mSF} and $g_{mCurrent\text{-}source}$ are the trans-conductance of the source follower and current source respectively. The trans-conductance g_{mSF} is proportional to transistor size for a given value of overdrive ($V_{GS}–V_T$). Reducing the output resistance by increasing the source follower transistor size has the detrimental effect of increasing the value of C_{in} and C_{SL} of the buffer resulting in a relatively low ratio of C_L/C_{in} for the required 3 dB bandwidth.

6.1.2 Source Coupled Differential Pair Based Unity Gain Buffer

An alternative topology for a unity gain buffer is based on a source coupled differential pair as shown in Fig 6.1.1 [45] [46]. The operation of the differential pair is based on the current generated by the common source current sink (M5) being split by matched differential pair M1 and M2 and the matched pair M3 and M4. Ignoring dynamic drain resistance, near unity gain will be obtained if $g_{m1} = g_{m2} = g_{m3} = g_{m4}$. The thresholds of M1 and M2 vary with input/output voltages due to the body effect. Also, the variation of the P-channel trans-conductance with large signal input and output signals do not match the variation of N-channel trans-conductance. Both of these effects will limit the buffer input range and linearity (gain accuracy). Reducing output resistance by increasing the size of M4 also requires that M1 be increased to maintain a match so the input capacitance of the buffer is increased. A feedforward modification is presented in [45] to improve gain accuracy; however, the proposed modification increases the difficulty to maintain all transistors operating in saturation for submicron implementations with low voltage V_{dd} technologies, thereby reducing the maximum input amplitude range.

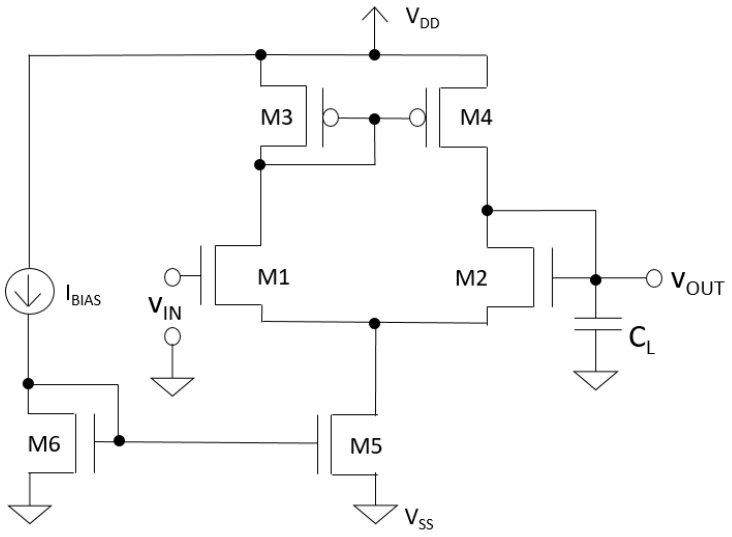

Fig 6.1.1 Source coupled differential pair unity gain buffer.

6.2 Two Stage Common Source Active Load Unity Gain Buffer

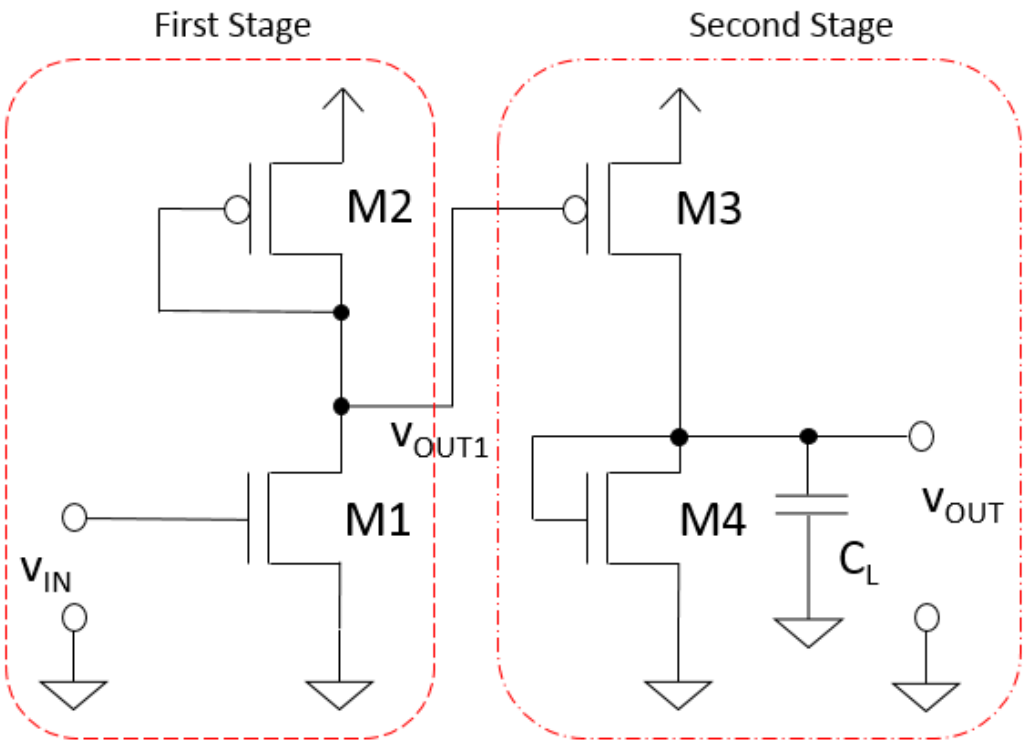

Fig 6.2.1 Two-stage CSAL analog buffer.

A two-stage common source active load (CSAL) unity gain buffer will be developed and analyzed to provide a basis for an improved buffer that is proposed in this section. The two-stage circuit is shown in Fig 6.2.1. The circuit is similar to the source coupled differential pair unity gain buffer discussed in section 6.1.2 except for the absence of the tail current source (M5). The circuit does not operate as a matched source coupled differential pair, but rather as a cascade of two common source amplifiers with active loads. Input biasing (offset) is provided by the driving circuit or realized with a capacitive coupled input with a high impedance voltage bias on the gate of M1. Output offset is set by adjusting the sizes of M3 and M4 relative to M1 and M2.

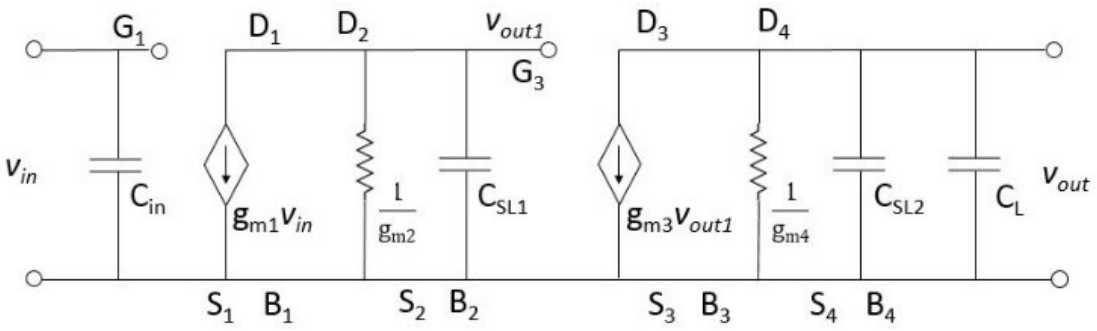

Fig 6.2.2 Two-stage CSAL linearized AC circuit

6.2.1 Linearized Small Signal Performance Analysis

The linearized AC equivalent circuit for the two-stage buffer is shown in Fig 6.2.2. The dynamic drain resistance has been ignored in the small signal equivalent circuit (r_{ds}>>1/g_m) to simplify the analysis and provide insight into the primary performance drivers.

From Fig 6.2.2, the transfer function is found to be

$$A_v(s) = \frac{v_{out}(s)}{v_{in}(s)} = \left(\frac{-\frac{g_{m1}}{g_{m2}}}{1+S\frac{C_{SL1}}{g_{m2}}}\right)\left(\frac{-\frac{g_{m3}}{g_{m4}}}{1+S\frac{C_{SL2}+C_L}{g_{m4}}}\right) \quad (6.2.1)$$

The product of the first and second stage gains (g_{m1}/g_{m2}) * (g_{m3}/g_{m4}) should be near 0 dB for unity gain. Note that there is no requirement for matching transistors for unity gain which provides flexibility in choosing transistor sizes based on buffer input capacitance requirements and maximizing the 3 dB bandwidth. The 3 dB bandwidth is determined by the two poles

$$P_1 = \frac{-g_{m2}}{C_{SL1}} \quad (6.2.2)$$

$$P_2 = \frac{-g_{m4}}{C_{SL1}+C_{SL}} \quad (6.2.3)$$

It is noted that stability is not an issue with this buffer since the gain of both stages is low.

The input capacitance presented by the CSAL buffer is approximated as

$$C_{in} \approx C_{gs1} + 2C_{gd1} \tag{6.2.4}$$

The output self-loading capacitance of the first stage is approximated by

$$C_{SL1} = C_{gs2} + C_{gs3} + C_{db2} + C_{db1} + C_{gd1} + C_{gd3} \tag{6.2.5}$$

And second stage self-loading capacitance is

$$C_{SL2} = C_{gs4} + C_{db3} + C_{db4} + C_{gb1} \tag{6.2.6}$$

The parasitic capacitance can be estimated by models which are proportional to gate widths [42]. Representative values in this dissertation are used below to facilitate first order analysis of the small signal linearized response.

$$C_{gs} \cong 1.0 \frac{fF}{\mu m} [W(\mu m)] \tag{6.2.7}$$

$$C_{gd} \cong 0.35 \frac{fF}{\mu m} [W(\mu m)] \tag{6.2.8}$$

$$C_{sb} = C_{db} \cong 0.6 \frac{fF}{\mu m} [W(\mu m)] \tag{6.2.9}$$

Also, the values of trans-conductance (g_m) can be approximated by Eq 6.2.10 and Eq 6.2.11 where it is seen that the values are not only a function of transistor widths, but also will vary with the overdrive (V_{GSQ}-V_{TN}) for $M1$ and $M4$ and (V_{SGQ}-$|V_{TP}|$) for $M2$ and $M3$, where V_{TN} and V_{TP} represent the threshold voltage of nmos and pmos transistor.

$$g_{mN} \cong K_{pN} \times \frac{W}{L} \left(V_{gs} - V_{TN}\right) \tag{6.2.10}$$

$$g_{mP} \cong K_{pP} \times \frac{W}{L} \left(V_{sg} - |V_{TP}|\right) \tag{6.2.11}$$

The problem becomes one of finding the combinations for $W1$, $W2$, $W3$, and $W4$ to maximize the bandwidth of the two-stage response under the unity gain constraint: (g_{m1}/g_{m2}) * (g_{m3}/g_{m4}) ≈ 1. A second constraint on the selection of W1 depends on the required value of C_{in}. Under the parasitic capacitance model, C_{in} ≈ 1.7 fF/μm * $W1$ (μm); so $W1$ (μm) is constrained to an approximate value of C_{in} (fF)/1.7 assuming the capacitance model above. As stated in Eq 6.2.2 and Eq 6.2.3, the two poles setting the

bandwidth are P_1 and P_2. C_{SL1} is typically much smaller than $C_{SL2} + C_L$, which implies choosing a relatively small g_{m2} and relatively large g_{m4}. A design procedure considering the above constraints is outlined below:

- Choose $W1$ based on the required value of C_{in}.
- Set the desired value of C_L.
- Choose a small value of $W2$ relative to $W1$ resulting in a relatively small value of g_{m2}.
- Set the input offset to the desired value (typically 0.6 V for 90 nm CMOS process with V_{dd} = 1.2 V)
- Use 90 nm process design kit with Cadence tools to select $W3$ and $W4$ to maximize the two stage 3 dB bandwidth with the two-stage low frequency gain near unity based on AC analysis.
- Iterate with additional values of $W2$ as needed. Produce Bode frequency plots for stage1, stage2, and two stage output response.
- Perform large signal transient analysis to make transistor size adjustments to obtain desired output offset and more accurately determine the low frequency gain, 3 dB bandwidth, and power dissipation.
- Perform large signal transient analysis to determine input dynamic range that yields a gain error of less than 2%.
- Perform transient analysis and FFT to determine THD.

6.2.2 CSAL Buffer Performance Analysis Based on 90 nm CMOS Design

The procedure outlined above is used to assess the performance of a 90 nm CMOS CSAL buffer design with $Cin \approx 5$ fF ($W1$ = 3 um) and C_L = 250 fF. The circuit is

designed for an input offset voltage of 0.6 V and output offset is approximate 0.6 V. The resulting transistor sizes are shown in Table 6.2.1.

The Bode plots (based on Cadence simulations) for stage 1, 2, and the output of 90nm CMOS CSAL buffer are shown in Fig 6.2.3. Referring to Fig 6.2.1, Stage 1 output is $20\log(v_{out1}/v_{in})$, Stage 2 output is $20\log(v_{out}/v_{out1})$, and Output is $20\log(v_{out}/v_{in})$. It is noted that the first stage transfer function has a low frequency gain of 4.28 dB and a 3 dB down bandwidth of 4.28 GHz which are relatively high because the loading is only the self-loading capacitance delineated in Eq 6.2.5. The second stage gain and 3 dB down bandwidth are -6.32 dB and 3.17 GHz with the 250 fF output load. The transistor sizes are adjusted as described in the previous procedure to obtain maximum output 3 dB bandwidth with a flat low frequency gain near 0 dB. The output result which is the product of stage 1 and 2 indicates a 3 dB bandwidth of 2.27 GHz and a low frequency gain of -2.04 dB. The –2.04 dB gain is accepted as a compromise to maximize 3 dB bandwidth.

Table 6.2.1 Transistor sizes of CSAL buffer optimized for 250fF capacitive load

Transistor	Width (μm)	Length (nm)
M1	3	100
M2	1	100
M3	12	100
M4	8	100

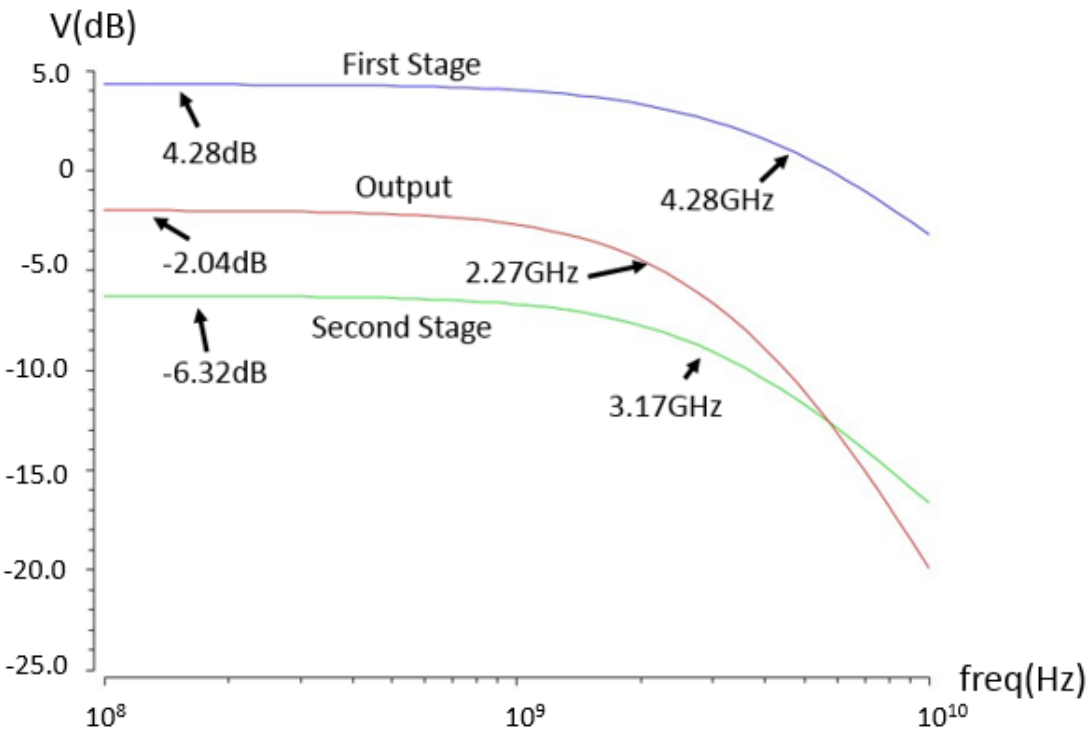

Fig 6.2.3 CSAL buffer AC analysis plot.

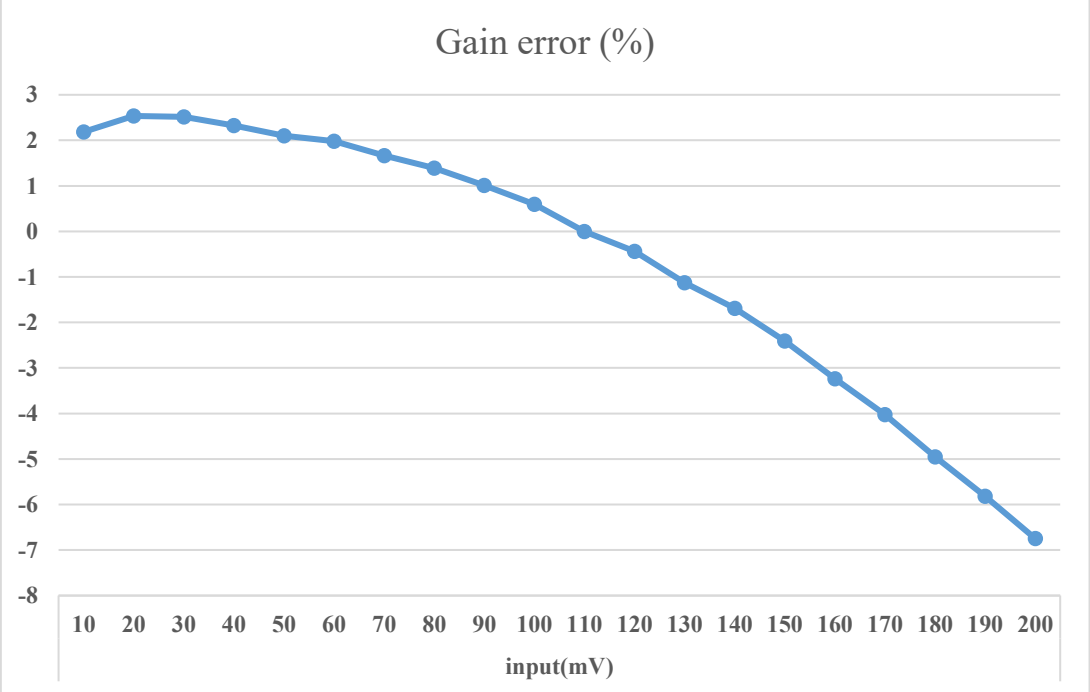

Fig 6.2.4 Gain error vs. input/output amplitude.

Table 6.2.2 Summary of single sided 90nm CMOS CSAL analog buffer performance optimized for 250fF load

Input Cap	Load Cap	Low Freq Gain	3dB BW	Input Range/ Gain Accuracy	THD	Input/Output Offset	Power
≈5fF	50fF	-2.79dB	3.79GHz	140mV/< 2% variation	-54.3dB	0.6V/0.7V	730µW
≈5fF	250fF	-3.23dB	2.27GHz	140mV/< 2% variation	-54.3dB	0.6V/0.7V	731µW

Transient analysis was performed to determine bandwidth, gain, output offset, gain accuracy THD, and power dissipation. A plot of variation in gain versus input amplitude is shown in Fig 6.2.4 indicating a maximum input amplitude with less than 2% gain variation of 140 mV when driving a 250 fF load, and the THD is -54.3 dB when assessed for the 250 fF load.

Performance of the CSAL analog buffer is summarized in Table 6.2.2 for the design optimized to drive 250 fF load when driving 250 fF and also when driving 50 fF. The results above indicate that the CSAL buffer has good 3 dB bandwidth for a relatively large ratio of output capacitive load to input capacitive load (C_L/C_{in}). However, some performance parameters need improvement.

(1) Large signal input magnitude range for a 2% gain accuracy is relatively small.

(2) THD needs improvement.

The two stage CSAL buffer discussed above uses a first stage with an active load P-channel pull up and an active load N-channel pull down on the second stage. It is difficult to obtain a symmetric result for rising and falling inputs and outputs causing limitations with regard to offset error, gain accuracy, and THD. These performance issues are improved by a proposed double sided CSAL analog buffer with source feedback.

6.3 Double Sided Active Load Analog Buffer with Source Feedback

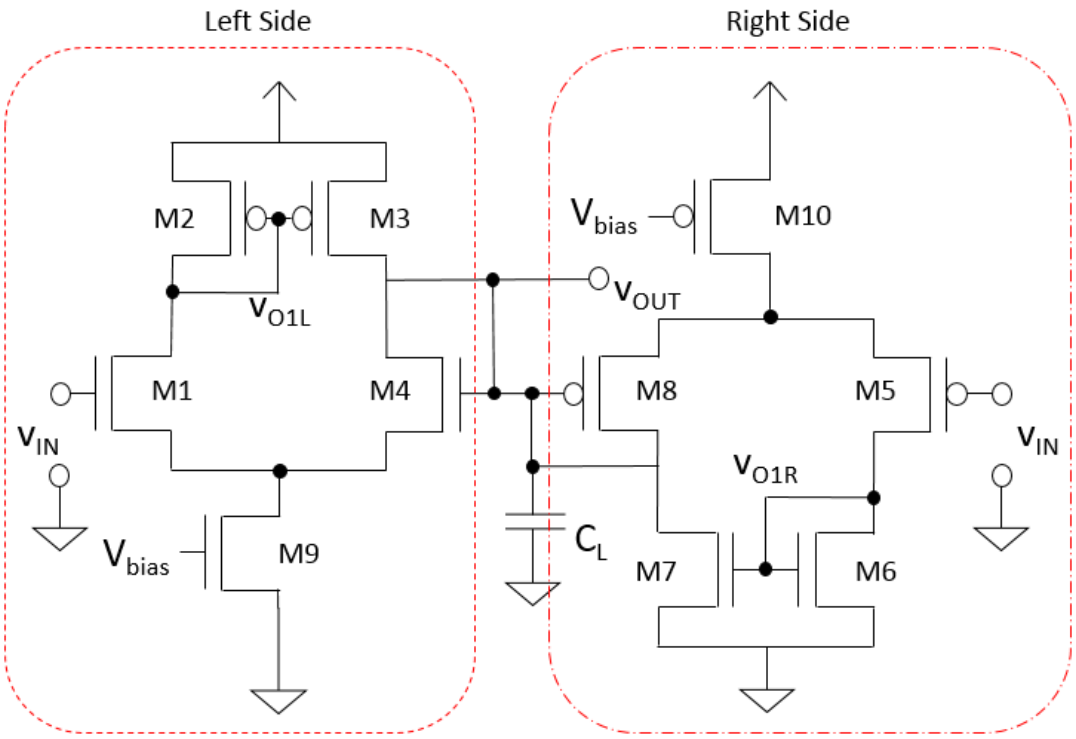

Fig. 6.3.1 Two stage CSAL buffer with source feedback.

A proposed two stage Double Sided Common Source Active Load (DSCSAL) analog buffer with source feedback is shown in Fig 6.3.1. Input biasing (offset) is provided by the driving circuit or realized with capacitive coupled input with a high impedance voltage bias on the gate of *M*1 and *M*5.

For this double-sided circuit, M9 and M10 are operating in the linear region with $V_{ds9}<V_{gs9}$ - V_{T9} ($V_{sd10}<V_{sg10}-|V_{T10}|$), so both transistors are modeled as resistors, $R_s \approx 1/\beta (V_{gs}-V_T)$ rather than a tail current source. Also, the parasitic self-loading capacitance at the source of M1 and M4 is $C_{SL} \approx C_{DB9}+C_{SB1}+C_{SB4}$. Similarly, a parasitic capacitance is formed at the source of M5 and M8, $C_{SR} \approx C_{DB10}+C_{SB5}+C_{SB8}$.

Thus, the result of adding M9 and M10 is a resistor/capacitor parallel combination at the source of M1 and M4 and the source of M5 and M8. The circuit can be implemented with M9 and M10 replaced by resistor/capacitor parallel pairs, but the

effective area is increased. It is important to note that M9 and M10 must operate in the linear region (not as current sources) to realize the performance described below. This is a key difference compared to a matched differential pair buffer.

The left side of the DSCSAL buffer is identical to the single sided CSAL buffer previously discussed except for the addition of M9. The right side mirrors the left side with p-channel transistors replaced by n-channel and vice versa. When the p-channel M2 is pulling up, the n-channel M6 is pulling down; when *M*4 is pulling down, M8 is pulling up. As will be seen the complementary actions of the two sides improves performance compared to the single sided circuit.

6.3.1 Linearized Small Signal Performance Analysis

The linearized AC equivalent circuit is shown in Fig 6.3.2. The dynamic drain resistances have been ignored in the small signal equivalent circuit since $r_{dsx}>>1/g_{mx}$.

To obtain insight into the operation of the DSCSAL buffer, a small signal transfer function will be developed for the case where the right side small signal parameters are equal to the left side parameters; that is: $g_{m1}=g_{m5}$; $g_{m2}=g_{m6}$; $g_{m3}=g_{m7}$; $g_{m4}=g_{m8}$; $C_{gs1}=C_{gs5}$; $C_{SL1}=C_{SR1}$; $C_{SL2}=C_{SR2}$; $C_{SL}=C_{SR}=C_S$; $R_{SL}=R_{SR}=R_S$;

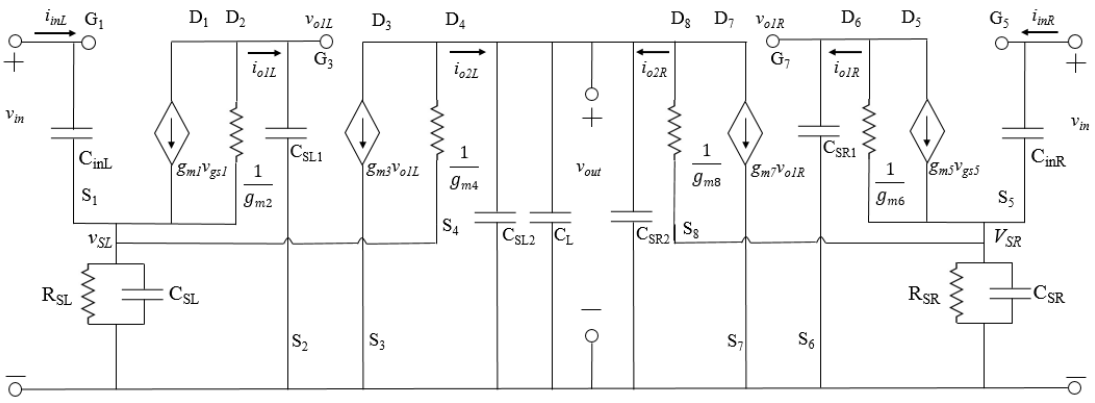

Fig. 6.3.2 Small signal model of DSCSAL buffer with source feedback

Then the first stage transfer function is:

$$\frac{v_{o1L}}{v_{in}} = \frac{v_{o1R}}{v_{in}} \tag{6.3.1}$$

Referring to Fig 6.3.1,

$$-i_{o1L} = g_{m1}v_{gs1} + g_{m2}(v_{o1L} - v_{SL}) \tag{6.3.2}$$

$$-i_{o1L} = g_{m1}(v_{in} - v_{SL}) + g_{m2}(v_{o1L} - v_{SL}) \tag{6.3.3}$$

$$-i_{o1L} = g_{m1}v_{in} + g_{m2}v_{o1L} - (g_{m1} + g_{m2})v_{SL} \tag{6.3.4}$$

For the input current:

$$i_{inL} = sC_{inL}v_{gs1} = sC_{inL}(v_{in} - v_{SL}) \tag{6.3.5}$$

Then the left side source voltage for $M1$ and $M4$ can be evaluated:

$$v_{SL} = \frac{-i_{o1L}+i_{inL}+g_{m4}(v_{out}-v_{SL})}{g_{m9}+sC_{SL}} \tag{6.3.6}$$

Eq 6.3.4 and Eq 6.3.5 into Eq 6.3.6 yields:

$$v_{SL} = \frac{(g_{m1}+sC_{inL})v_{in}+g_{m2}v_{o1L}+g_{m4}v_{out})}{(g_{m9}+g_{mx})+s(C_{inL}+C_{SL})} \tag{6.3.7}$$

Where $g_{mx}=g_{m1}+g_{m2}+g_{m4}$.

Eq 6.3.7 and Eq 6.3.4 yields:

$$-i_{o1L} = \left[g_{m1} - (g_{m1} + g_{m2})\left(\frac{g_{m1}+sC_{inL}}{A+sB}\right)\right]v_{in} + \left[g_{m2} - (g_{m1} + g_{m2})\left(\frac{g_{m2}}{A+sB}\right)\right]v_{o1L} -$$

$$\left[(g_{m1} + g_{m2})\left(\frac{g_{m2}}{A+sB}\right)\right]v_{out} \tag{6.3.8}$$

Where $A=g_{m9}+g_{mx}$, and $B=C_{inL}+C_{SL}$.

The first stage output v_{o1L} is

$$v_{o1L} = i_{o1L}\left(\frac{1}{sC_{SL1}}\right) \tag{6.3.9}$$

Substituting Eq 6.3.8 in Eq 6.3.9 yields (after some work)

$$\frac{v_{o1L}(s)}{v_{in}(s)} = \frac{G_{o1}\left(1+\frac{s}{Z_{o1}}\right)+G_1\left(\frac{v_{out}}{v_{in}}\right)}{1+\frac{s}{\omega_{o1}Q_{o1}}+\frac{s^2}{\omega_{o1}{}^2}} \tag{6.3.10}$$

Where

$$G_{o1} = -\frac{g_{m1}}{g_{m2}}$$

$$G_1 = \frac{\frac{g_{m4}}{g_{m9}}(g_{m1}+g_{m2})}{g_{m2}(1+\frac{g_{m4}}{g_{m9}})}$$

$$Z_{o1} = \frac{g_{m4}+g_{m9}}{C_s-\frac{g_{m2}}{g_{m1}}C_{inL}}$$

$$\omega_{o1} = \sqrt{\frac{g_{m2}(g_{m4}+g_{m5})}{(C_{inL}+C_S)C_{SL1}}}$$

And the value of $\omega_{o1}Q_{o1}$ is:

$$\frac{g_{m2}(g_{m4}+g_{m9})}{(g_{m1}+g_{m2}+g_{m4}+g_{m9})C_{S4}+(C_{inL}+C_S)g_{m2}}$$

For $s\rightarrow 0$, and $v_{out}/v_{in}\,(s=0)=1$, the low frequency gain is:

$$\frac{v_{o1L}}{v_{in}}(s=0) = G_{o1} + G_1\left[\frac{v_{out}}{v_{in}}(s=0)\right] = G_{o1} + G_1 \qquad (6.3.11)$$

For $g_{m9}\rightarrow\infty$ and $C_s\rightarrow 0$ (no tail transistors), Eq 6.3.10 yields the expected result for the first stage active load amplifier.

$$\frac{v_{o1L}}{v_{in}} = \frac{-\frac{g_{m1}}{g_{m2}}}{[1+s(\frac{C_{SL1}}{g_{m2}})} \qquad (6.3.12)$$

It is seen from Eq 6.3.10 that v_{o1L}/v_{in} is dependent on v_{out}/v_{in} due to the feedback from the output (via source of $M4$) to the source of $M1$.

For the second stage, again referring to Fig 6.3.1

$$-i_{o2L} = g_{m3}v_{o1L} + g_{m4}(v_{out} - v_{SL}) \qquad (6.3.13)$$

Substituting Eq 3.3.7 into Eq 6.3.13 yields:

$$-i_{o2L} = \left[\frac{g_{m3}-Kg_{m2}+sg_{m3}D}{(1+sD)}\right]v_{o1L} + \left[\frac{g_{m4}-Kg_{m4}+sg_{m4}D}{(1+sD)}\right]v_{out} - \left[\frac{Kg_{m1}+sC_{inL}K}{(1+sD)}\right]v_{in} \quad (6.3.14)$$

Where K=$g_{mx}/(g_{m9}+g_{mx})$, and D=$(C_{inL}+C_S)/(g_{m9}+g_{mx})$.

The output voltage is determined by output current from both the left and right sides which results in a factor of two for the current driving the total output capacitance C_T.

$$v_{out} = 2i_{o2L}\left(\frac{1}{sC_T}\right) \tag{6.3.15}$$

Where C_T=C_{SL2}+C_L+C_{SR2}.

Combine Eq 6.3.14 and Eq 6.3.15 yields the second stage small signal response (after some work)

$$\frac{v_{out}(s)}{v_{o1L}(s)} = \frac{G_{o2}\left(1+\frac{s}{Z_{o2}}\right)+G_2\left(1+\frac{s}{Z_2}\right)\frac{v_{in}(s)}{v_{o1L}(s)}}{1+\frac{s}{\omega_{o2}Q_{o2}}+\frac{s^2}{\omega_{o2}{}^2}} \tag{6.3.16}$$

Where

$$G_{o2} = -\frac{-g_{m3}+Kg_{m2}}{g_{m4}(1-K)}$$

$$G_2 = -\frac{Kg_{m1}}{g_{m4}(1-K)}$$

$$Z_{o2} = -\frac{g_{m3}-Kg_{m2}}{g_{m3}D}$$

$$Z_2 = \frac{g_{m1}}{C_{inL}}$$

$$\omega_{o2} = \sqrt{\frac{2g_{m4}(1-K)}{DC_T}}$$

$$\omega_{o2}Q_{o2} = \frac{2g_{m4}(1-K)}{2g_{m4}D+C_T}$$

$$D = \frac{C_{inL}+C_S}{g_{m1}+g_{m2}+g_{m4}+g_{m9}}$$

$$C_T = C_L + C_{SL2+CSR2}$$

For s→0, the low frequency gain is:

$$\frac{v_{out}}{v_{o1L}}(s=0) = G_{o2} + G_2\left[\frac{v_{in}}{v_{o1L}}(s=0)\right] = G_{o1} + \frac{G_2}{G_{o1}+G_1} \tag{6.3.17}$$

For g_{m5}→∞ and C_S→0 (no tail transistors), Eq 6.3.16 collapses to the expected second stage active load result:

$$\frac{v_{out}}{v_{o1L}} = \frac{-\frac{g_{m3}}{g_{m4}}}{[1+s(\frac{2C_{SL1}+C_{SL}}{2g_{m4}})} \tag{6.3.18}$$

It is seen from Eq 6.3.17 that v_{out}/v_{o1L} is dependent on v_{o1L}/v_{in} due to the feed ward

from the input (via source of $M1$) to the drain of $M4$ (output).

The first stage transfer function in Eq 6.3.10 shows that the addition of the tail transistors in the DSCSAL buffer results in second order pole response in the denominator and the addition of a zero in the numerator. The values of ω_{o1}, Q_{o1}, and Z_{o1} can be adjusted to not only increase the first stage frequency response, but also to interact with the second stage response to obtain a unity gain buffer with a significantly increased 3dB bandwidth. Specifically, the Q_{o1} is adjusted so that the first stage is underdamped with a modest peak frequency response. The second stage response given by Eq 6.3.16 also has a second order response in the denominator; however, the relatively large load capacitance (C_L) results in a small Q_{o2} with over damping. The proper selection of parameters results in the combination of the first stage underdamped response and the second stage over damped response producing a flat output (v_{out}/v_{in}) frequency response with higher bandwidth.

From Fig 6.3.1, it is seen that the addition of the transistors operating in the resistive mode results in a reduction in the magnitudes of v_{gs1} and v_{sg5} for the input transistors creating degenerative source feedback for the first stage of both sides. Degenerative source feedback has the effect of mitigating the non-linear effects of the large signal variation at the input [47]. It is also noted that the source of the second stage output active load transistors $M4$ and $M8$ are also connected to the feedback node (drains of $M9$ and $M10$) resulting in degenerative source feedback from the second stage output nodes. The source feedback on the output active loads results in a more linear output active resistor magnitude ($1/g_m$) as the output signal magnitude increases. The net effect is to improve the large signal linearity (input range/gain accuracy) as a result of the degenerative source feedback. This result will be demonstrated in the next section where the proposed DSCSAL analog buffer with source feedback is designed in 90nm

CMOS technology.

6.3.2 DSCSAL Buffer with Source Feedback Performance Analysis Based on 90 nm CMOS Design

The DSCSAL circuit with source feedback is designed using 90 nm CMOS technology to assess performance with Cadence tools. The buffer is initially designed using schematic for assessing performance and optimizing transistor sizes followed by layout and performance assessment based on layout extraction including RC parasitic. The resulting layout for the DSCSAL buffer with source feedback is shown in Fig 6.3.3.

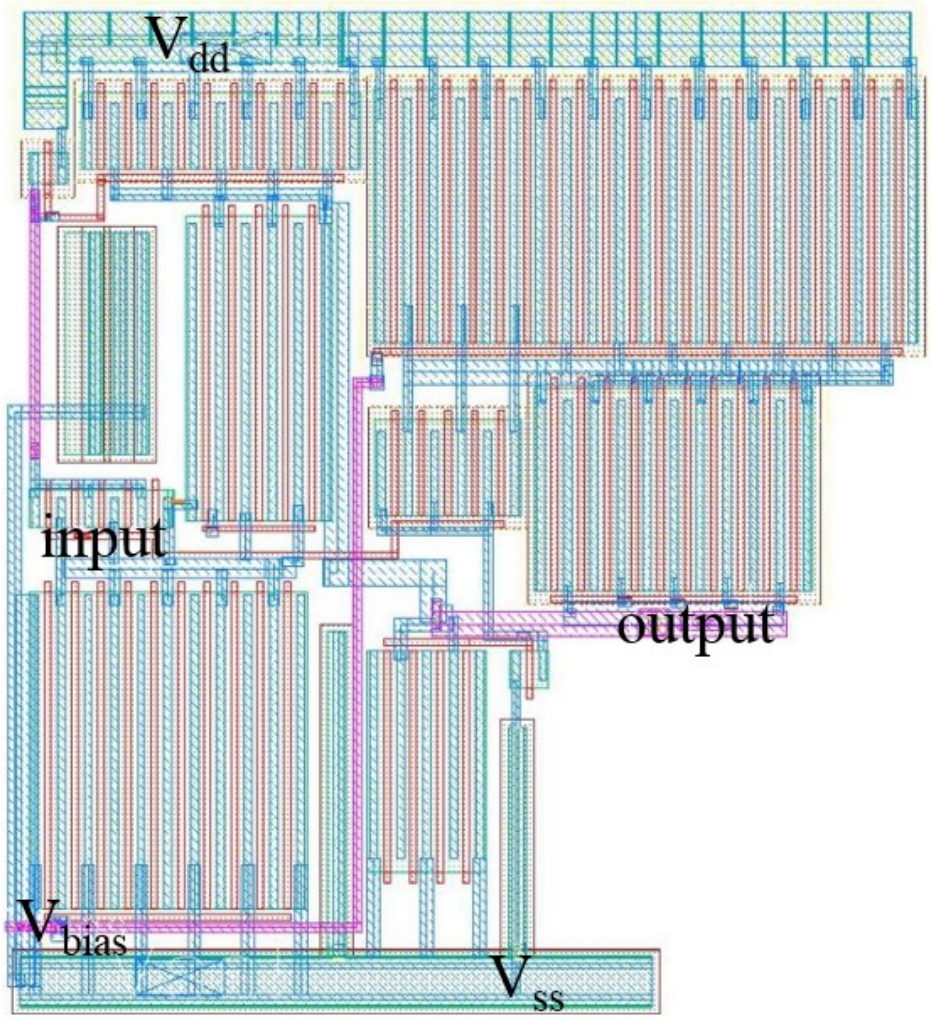

Fig. 6.3.3 Layout of proposed DSCSAL buffer

Table 6.3.1 is the transistor sizes for the proposed DSCSAL buffer with feedback transistors optimized for driving 250 fF output load.

The Bode frequency plots for stage 1, 2, and the outputs are shown in Fig 6.3.4, which indicate a 3 dB bandwidth of 4.4 GHz and a low frequency gain of 0.16 dB output response.

In Fig 6.3.4 the right and left side first stage plots are the frequency response of $v_{o1R}(s)/v_{in}(s)$ and $v_{o1L}(s)/v_{in}(s)$. Note the second order result as previously discussed with the under damped response showing a peak magnitude in the vicinity of 4 GHz.

The $v_{out}(s)/v_{in}(s)$ frequency result combines the two stage transfer functions that have been shaped by selecting the proper sizes of the transistors to obtain maximize 3 dB bandwidth with a flat unity gain. The right and left side second stage plots are the $v_{out}(s)/ v_{o1R}(s)$ and $v_{out}(s)/ v_{o1R}(s)$ results with the overdamped second order response.

Table 6.3.1 Transistor sizes of DSCSAL Analog Buffer optimized for 250 fF capacitive load

Transistor	Width (μm)	Length (nm)
M1	3	100
M2	0.5	100
M3	5	100
M4	16	100
M5	7.5	100
M6	0.6	100
M7	7	100
M8	24	100
M9	50	100
M10	80	100

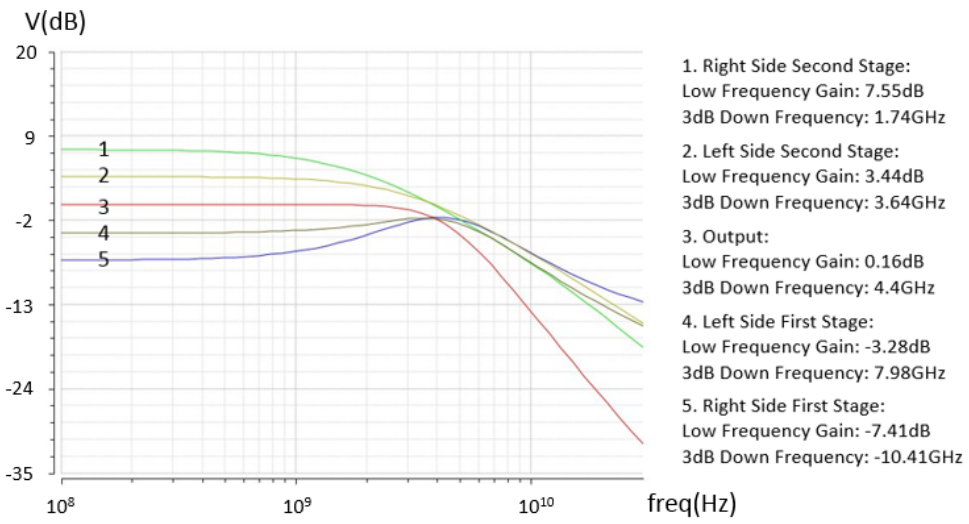

Fig. 6.3.4 AC analysis plots of DSCSAL buffer.

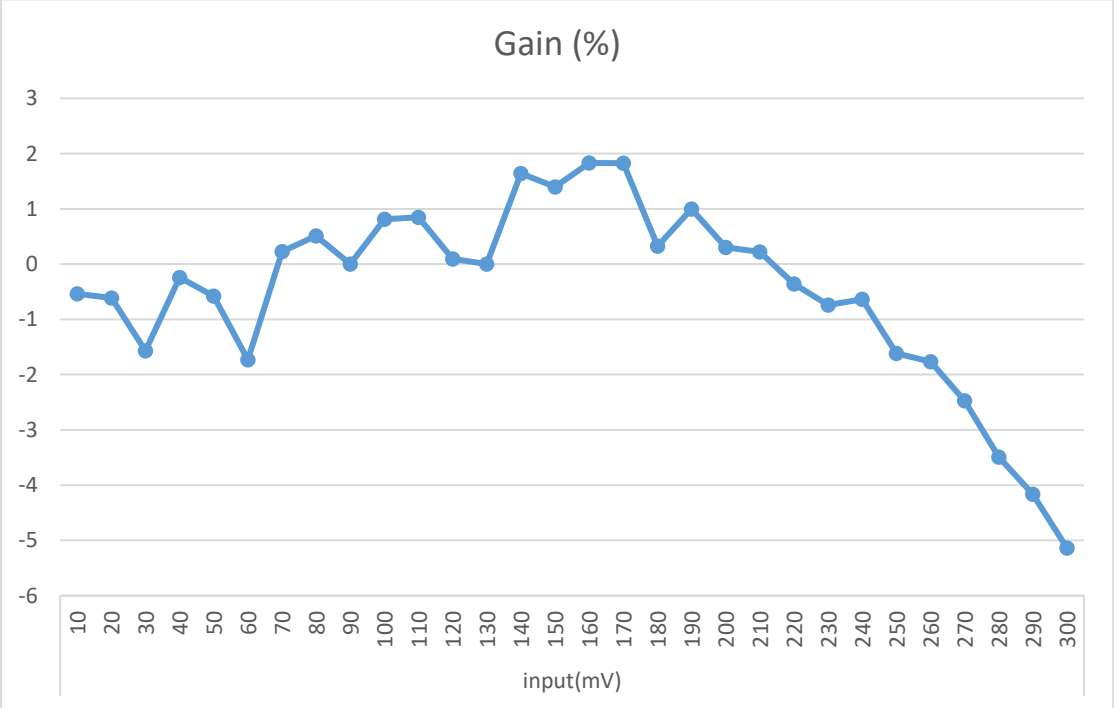

Fig. 6.3.5 Gain Error vs Input/Output Amplitude

Table 6.3.2 Summary of single sided 90 nm CMOS Double Sided CSAL Analog Buffer with Source Feedback Performance Optimized for 250 fF load

Input Cap	Load Cap	Low Freq Gain	3dB BW	Input Range/ Gain Accuracy	THD	Input/Output Offset	Power
≈10fF	50fF	0.16dB	6.43GHz	270mV/ <2% variation	-63.3dB	0.6V/0.57V	1025uW
≈10fF	250fF	0.16dB	4.4GHz	270mV/ <2% variation	-63.3dB	0.6V/0.57V	1058uW

Large signal transient analysis was performed to determine low frequency gain, output offset, gain accuracy, THD, and power dissipation. A plot of variation in gain verses input amplitude is shown in Fig 6.3.5 indicating a maximum input amplitude with less than 2% gain variation of 260 mV when driving a 250 fF load. The total harmonic distortion is -63.3 dB when assessed for the 250 fF load.

Performance of the DSCSAL analog buffer is summarized in Table 6.3.2 for 250 fF and 50 fF loads. It is noted that the transistor sizes are selected to optimize performance for the 250 fF load.

Comparing the single sided CSAL buffer performance in Table 6.2.2 to the DSCSAL with source feedback in Table 6.3.2, it is seen that all parameters of performance have significant improvements. The cost is some increase in input capacitance, layout size and power consumption.

6.4 Comparison to Other Published Work

A comparison of the proposed DSCSAL buffer with source feedback to other published unity gain buffers is shown in Table 6.4.1.

Table 6.4.1 Comparison of the proposed DSCSAL with source feedback to other published unity gain buffers

Load Cap	Design	Tech	Low Freq Gain	3dB BW	Input Range/Gain Accuracy	THD	Offset Error	Power
13pF	[42]	0.35um	-0.13dB	87MHz	---/ <1.8% variation	-59dB	29mV	4.8mW
	This Work	***90nm***	***0.17dB***	***153MHz***	***270mV/<2% variation***	***-63.7dB***	***26mV***	***1.06mW***
1pF	[43]	0.35um	-0.14dB	100MHz	---/<1.6% variation	-60dB	----	----
	This Work	***90nm***	***0.09dB***	***1.97GHz***	***270mV/<2% variation***	***-63.3dB***	***26mV***	***1.06mW***
2pF	[45]	1.2um	----	19MHz	-----	-60dB	72mV	0.45mW
	This Work	***90nm***	***0.34dB***	***1.07GHz***	***270mV/<2% variation***	***-63.3dB***	***26mV***	***1.06mW***

Previous work that was found was based on CMOS technologies with larger feature sizes driving larger capacitive loads. To provide a comparison, the DSCSAL buffer performance was assessed when driving the same capacitive load reported in each of the previous published work. As seen in Table 6.4.1, the DSCSAL buffer has a significantly increased 3 dB bandwidth for each comparison even though the proposed buffer was designed to optimize performance with a 250 fF load. Other performance parameters are comparable or improved for the proposed buffer (where data permitted comparisons). A key parameter missing for other published work was the input capacitance.

6.5 Conclusion

A proposed double sided common source active load unity gain buffer with source feedback implemented in 90 nm CMOS technology. This buffer has a very wide unity

gain 3dB bandwidth of 4.4 GHz with an output to input capacitive load ratio of 250 fF/10 fF. This design (optimized for the 250 fF load) has a 3dB bandwidth of 6.43 GHz for a 50 fF load and 1.97 GHz for a 1 pF load. The double sided design together with degenerative source feedback provides a large input/output voltage range while maintaining a less than 2% variation in gain for input amplitudes up to 270 mV. The total harmonic distortion is -63.3 dB. The double sided design provides flexibility in choosing transistor sizes to obtain unity gain with minimal offset error over a very wide bandwidth. The active load, low gain design eliminates stability issues with no requirement for a compensation capacitor to create a dominate pole which results in reduced bandwidth. The V_{dd} to V_{ss} path includes an active load diode connected transistor, a common source transistor, and a degenerative source transistor acting as a resistor with very low drain to source voltage drop. This topology facilitates keeping the common source transistors in the saturation mode thereby making the buffer architecture suitable for submicron CMOS technologies with low rail voltages. The proposed new buffer architecture is an attractive option for on-chip submicron CMOS applications requiring a very wide unity gain bandwidth, large C_L/C_{in} ratio and excellent gain accuracy over a large input/output dynamic range.

VII. On-chip Self-Calibration System for CMOS Active Inductor Band Pass Filter

(The discussion in the following chapter is substantially drawn from [29], where we first reported the development and evaluation of this technique.)

7.1 Introduction

From the content of chapter 4, the process variation has a huge impact on AIBPF circuit performance. In order to maintain the active filter operating with designed specification after fabrication, the post-fab calibration technique must be implemented to compensate the process variation. Previous work have addressed either off chip post fabrication calibration techniques for correcting AIBPF center frequency and Q values [15] [32]or self-compensation solution for low frequency base band active filter design [48]. This chapter is focused on an on-chip self-calibration system for higher RF frequency AIBPFs. The objective is to develop a relatively straight forward technique that operates at RF frequencies with a relatively high payoff post fabrication functionality. The proposed system can capture the center frequency error, analyze variation type, and compensate process variation automatically.

7.2 Process Variation Detection and Calibration

The on-chip self-calibration system should have the following functions. 1) Determine post fabrication center frequency that has been altered by process variation/mismatch; 2) Provide a mechanism to tune the center frequency to the desired value; 3) Maintain the corrected center frequency after calibration process. The proposed design is based on the principle that the amplitude of the AIBPF output should be the largest at the desired center frequency as shown in Fig 7.2.1. Three sine wave signals are generated with the same amplitude: signal 1 at a frequency $f_L = f_C - f_{6dB}$,

signal 2 at a frequency f_C and signal 3 at a frequency $f_H = f_C + f_{6dB}$. The three signals are sequentially applied in short bursts to the input of the AIBPF with the sequence repeated 14 times. A peak detector converts the AIBPF output amplitude for each of the three signals to three different DC signals which are fed to the following comparator sequentially. The peak amplitude DC value converted from the f_C input signal is stored by a track and hold circuit as reference data that is then compared with other two DC signals. For each sequence of input signals, on-chip logic determines which of the three peak detector signals is the largest to facilitate incrementally adjusting the bias control in the proper direction to bring the desired frequency (f_C) to be located between f_L and f_H. The feedback mechanism shown in Fig 7.2.1 operates to adjust V_{Bias1} and V_{Bias2} in opposite directions sequentially to incrementally approach a stable condition with the desired center frequency. Changing both bias voltages in this manner resulted in a faster convergence compared to fixing one and changing the other. This technique also had the effect of minimizing the change in gain and Q of calibrated filter compared to the prefabricated design values. The change of bias voltages is accomplished by charge pumps that receive up or down pulses from the logic circuitry during each sequence of the three inputs.

If process variation effects are minimal, the AIBPF has maximum amplitude at the center frequency as shown in Fig 7.2.2(a). Then the logic circuitry produces 0 on both up and down inputs to the charge pumps and bias controls are unchanged. This is repeated for the 14 repetitions of the three input signals with no change at the end of the sequence. If the post fab process parameters have shifted towards the slow corner, relative positions of f_L, f_C, and f_H are as presented in Fig 7.2.2(b). In this case, the comparator generates a pulse signal associated with the slow corner indicator while keeping a 0 at the fast corner indicator. The pulse signal causes a 1 to be sent to the up

input of charge pump 1 and to the down input of charge pump 2 in Fig 7.2.1. The output value of both charge pumps is changing, and the V_{Bias1} and V_{Bias2} of AIBPF are compensated to move the AIBPF center frequency toward the desired value. After a sequence of 14 input signals, the resulting bias voltage will have placed f_c in the middle and the bias value is held constant until next calibration process.

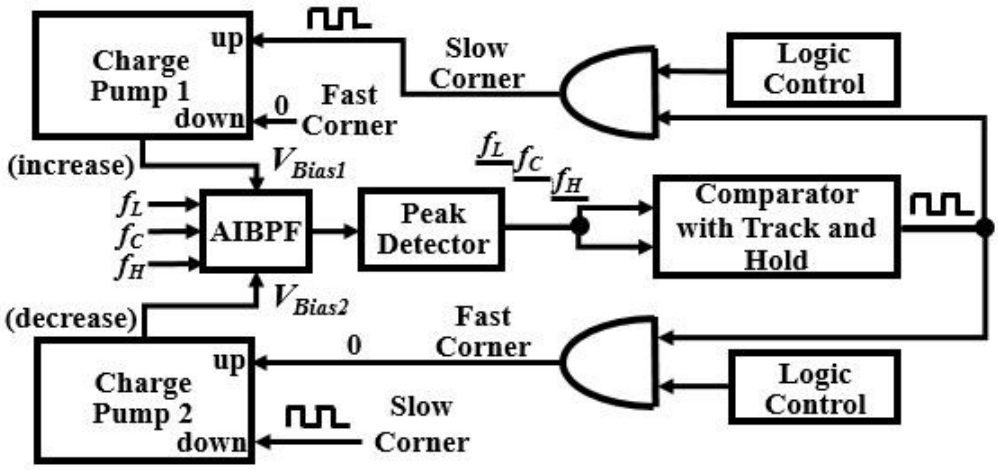

Fig 7.2.1 Proposed calibration system block diagram of AIBPF

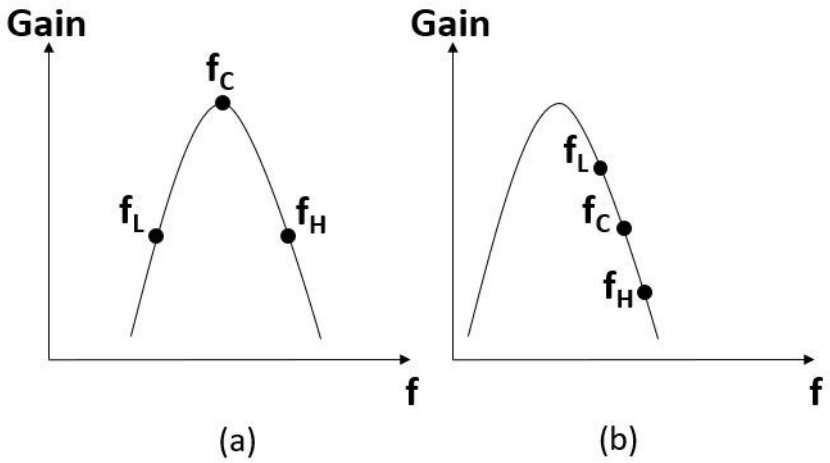

Fig 7.2.2 Process variation effect of AIBPF: (a) Without process variation (b) With process variation (process parameters towards the slow corner

The current implementation employs an off chip Arbitrary Wave Generator (AWG) to generate the desired three input signals (50 ns CW burst at f_L, 100 ns CW burst at f_C, and 50 ns CW burst at f_H) which is repeated 14 times to allow convergence to a bias signal value that will place the fc signal at the peak output amplitude.

The on-chip calibration circuitry should draw as little power as possible when the AIBPF is operating on line (not in calibration mode). To realize this goal, a virtual power structural [49] is employed in most circuit blocks of the calibration system. In calibration mode, the virtual power transistor is turned on, and delivers supply power to the calibration system. If calibration control switch is off, all calibration system circuits with virtual power structural are shut down by turning off the virtual power transistors, and the power consumption caused by leakage current of all additional circuits is very small compared to AIBPF.

7.3 Charge Pump

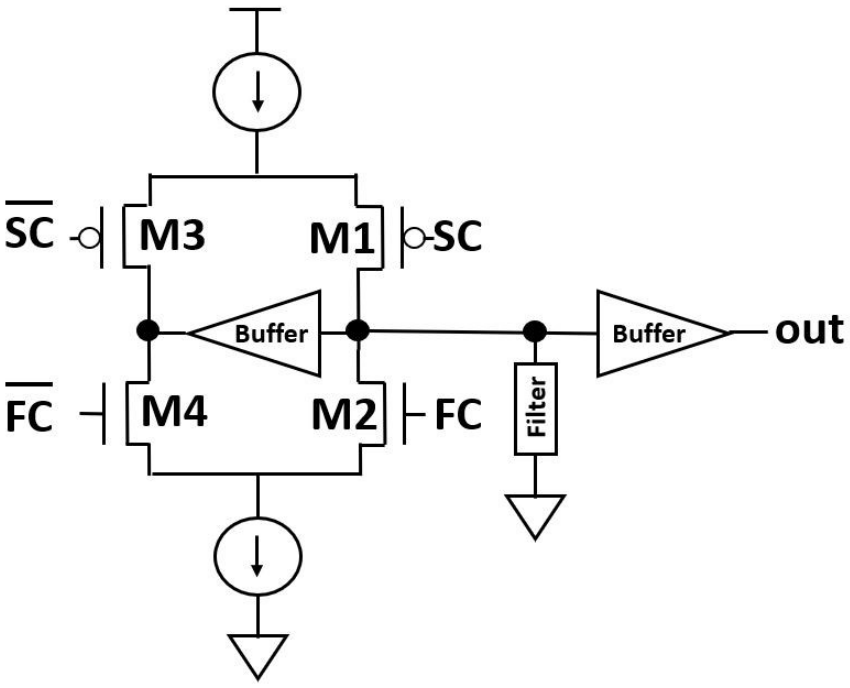

Fig 7.3.1 Charge pump schematic diagram

A standard charge pump [50] shown in Fig 7.3.1 is used to provide and change the voltage of V_{Bias1} and V_{Bias2} by SC (slow corner) and FC (fast corner) signals as discussed in Section 3. Since the AIBPF is very sensitive with bias voltage changing, the current flowing through M1 and M2 must be very small to have fine output changing step size. As shown in Table 7.3.1, the width of M1 to M4 is already close to the minimum value. To further decrease the output voltage changing step size, the transistor lengths are increased to 5 μm.

Tabel 7.3.1 Components parameter in charge pump

Component	Width (μm)	length (μm)
M1	0.5	5
M2	0.12	5
M3	0.5	5
M4	0.12	5

7.4 Simulation Results

To demonstrate performance, a 5.25 GHz center frequency AIBPF with on-chip self-calibration system is designed using 90 nm CMOS technology. The AIBPF is using the one designed in chapter 4. Process variation is simulated by Monte Carlo analysis with 20 sampling points. Based on the operation presented in the previous section, the sequence of 3 signals with same amplitude but different frequencies (5 GHz, 5.25 GHz, and 5.5 GHz) are the inputs to the AIBPF during calibration. If process variation has a minimal effect, the 5.25 GHz frequency output of filter has the largest amplitude, and the bias input remains unchanged during calibration process. Otherwise, one of the other two test signals (5 GHz and 5.5 GHz) will generate the largest output amplitude of the AIBPF. The top waveform at the first iteration of Fig 7.4.1 shows 5 GHz (f_L) signal amplitude is the largest among three test signals where process variation has

shifted the filter operation towards slow corner. The calibration system collects this information and generates pulse signals to the up node and down node of charge pump 1 and 2, respectively. These signals result in the changing of V_{Bias1} and V_{Bias2}, so that the center frequency is adjusted in an iterative manner during calibration period. At the end of the test sequence, the 5.25 GHz output regains the largest amplitude, and the final compensated bias value is stored by charge pump and the calibration process is turned off. The AIBPF uses this new bias voltage value to obtain the 5.25 GHz targeted center frequency until the calibration is reactivated.

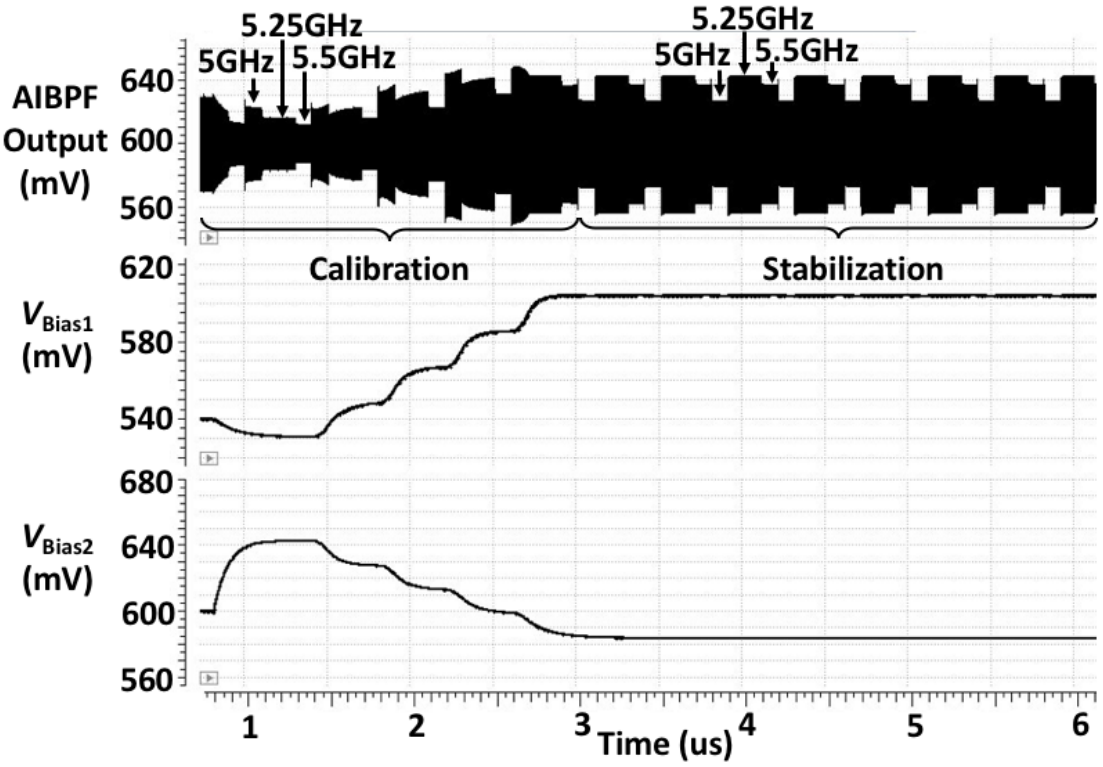

Fig 7.4.1 Cadence simulation result of AIBPF output and two bias voltages using proposed calibration system with slow corner process variation

Table 7.4.1 AIBPF simulation results

Parameters	Pre-fabrication	Post-fab before calibration	Post-fab after calibration
Center Frequency	5.25 GHz	5.86 GHz	5.26 GHz
Gain	28.8 dB	41.6 dB	37.9 dB
Bandwidth	140 MHz	40 MHz	50 MHz
Quality Factor (Q)	37.5	146	105
Linearity (input amplitude)	≤ 1.5 mV	≤ 200 μV	≤ 400 μV
Dynamic Range	34.17 dB	29.8 dB	29 dB

The results for a typical filter design sequence is summarized in Table 7.4.1, where the key filter parameters are shown for 1) prefabrication filter designed to specifications with typical PDK model parameters, 2) post fabrication performance prior to calibration based on a typical Monte Carlo process variation iteration, 3) post fabrication performance after calibration. The linearity parameter is the maximum sine voltage amplitude based on the 1 dB compression point and dynamic range is the maximum RMS sine wave amplitude divided by the RMS in band noise. As seen in Table 7.4.1, the desired center frequency has been obtained as a result of the calibration sequence. However other key parameters for the post fabrication filter have changed due to process variations and calibration adjustments to V_{Bias1} and V_{Bias2}. The gain and Q increase with a corresponding decrement in bandwidth and linearity compared to the prefabricated design. For some applications the increased gain and Q and reduced bandwidth may be a plus; however, the designer may have to incorporate additional flexibility in the design to adjust gain, Q, and bandwidth after calibration. Previous work has addressed incorporating mechanisms in the AIPBF design for adjusting post fabrication gain, Q, and bandwidth [15].

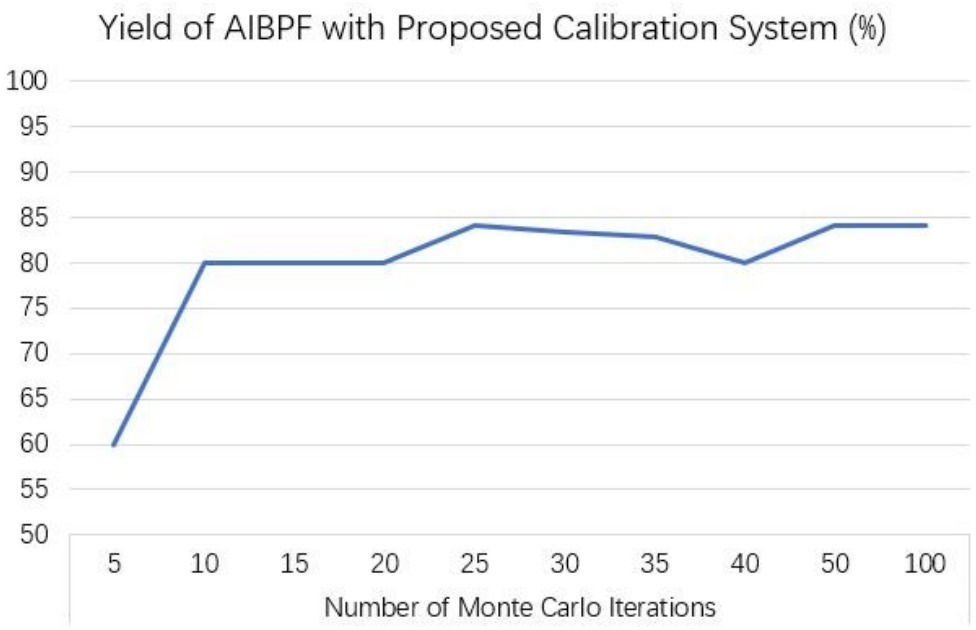

Fig 7.4.2 Yield versus number of Monte Carlo iterations with proposed calibration system

Among the 20 Monte Carlo analysis sampling results, there are 15 cases where the center frequency needs adjusting due to the process variations. With this number, the yield (ratio of good circuits to total fabricated circuits) for uncalibrated circuits is only 5/20 = 25%. Within these incorrect function results, the proposed calibration system successfully corrects 11 of them by adjusting the biases automatically, and the rate of finished product yield is increased to 16/20 = 80%. The 4 cases where calibration is not successful is due to a significant reduction in filter gain due to process variation. The filter response for all three calibration frequencies is so low that the calibration system cannot detect the difference in amplitude resulting in no change for a calibration run. This significant improvement in yield can lower the cost of fabrication and allows users to have the ability to restore the AIBPF center frequency when needed after chip is fabricated.

Table 7.4.2 Power consumption of proposed self-calibration system

Average power at slow corner	Calibration On	Calibration Off
AIBPF	3.7 mW	3.7 mW
Charge Pump	0.181 mW	0.183 mW
Other Self-Calibration Circuits	0.523mW	0.003mW

To show that 20 Monte Carlo iterations is sufficient to give an accurate estimate of yield, a plot of yield versus number of Monte Carlo iterations is shown in Fig 7.4.2 with number of iterations simulated up to 100. From the figure, the yield is between 80 and 84% for iterations more than 10. Therefore, 20 Monte Carlo seeds was considered sufficient to give a reasonably accurate estimate of yield.

The power consumption of AIBPF and proposed self-calibration system is listed in Table 7.4.2 when operating at 5.25 GHz desired center frequency. During calibration process, the calibration system consumes 0.704 mW extra power (Charge Pump plus Other Self-Calibration Circuits), which is 0.704 mW/3.7 mW = 19% of AIBPF power consumption. The charge pumps continue to operate when calibration is off, since charge pumps are used to supply and maintain the bias voltage. The other self-calibration circuitries require only 0.003 mW power when virtual power transistors are turned off during normal operation. The calibration system consumes 0.186 mW power when calibration is off, which is 5% of AIBPF power consumption.

7.5 Conclusion

A novel on-chip calibration system aimed at automatically compensating for the post fabrication process variation effects on 5.25 GHz active inductor band pass filters is presented in this chapter. The system is designed to correct the center frequency error by detecting the filter output amplitude and adjust bias voltages of AIBPF. The results

of 20 Monte Carlo analysis simulation run indicates the calibration system successfully relocates the center frequency at the desired value for most of the expected post fabrication process variations to be encountered. The rate of finished products yield is boosted from 25% to 80% by incorporating the proposed calibration system with AIBPF. Since all the circuits are constructed without passive inductors, the potential for higher Q and gain while operating at RF frequency are still preserved, and the total area consumption of AIBPF plus proposed self-calibration system is still much smaller than single stage passive inductor band pass filter with the same center frequency. Also, the virtual power technique guarantees the proposed calibration system adds relatively small power consumption to AIBPF when calibration mode is off.

VIII. Mixer

8.1 Introduction

In CMOS receiver chain system, mixer is an essential circuit block due to its frequency translating function. In most cases, the information sending out from transmitter is coupling on high frequency carrier signal to improve the propagation capability. This carrier frequency is created by Local Oscillator (LO), and it is also sent to receiver for frequency conversion. However, at receiver side, due to the circuit complexity and power consumption, the signal sending into ADC must have carrier signal removed, and this task is completed by mixer circuit in front end design.

As stated in chapter 2, both Hartley and Weaver frequency conversion systems can reject the image and improve the signal quality. The Hartley system only needs one Single-Input Differential-Output (SIDO) mixer simplified from Gilbert design at each path and one 90-degree shifter built in one path to perform the image rejection function. The Weaver architecture employs two mixers in each frequency shifting path to demodulate the wanted signal and remove the image part as demonstrated in Fig 8.1.1. A SIDO mixer is placed in the first stage to be compatible with the output from amplifier in Fig 2.1.6. The Gilbert mixer is used as the second stage down-converting component as its differential inputs can provide high gain to improve the output signal amplitude.

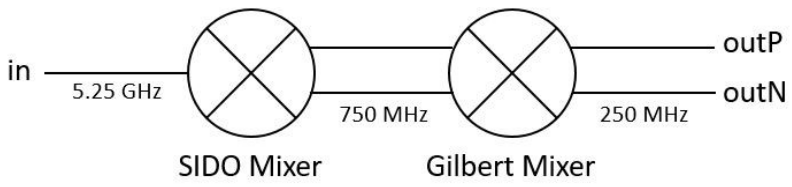

Fig 8.1.1 Frequency down-converting path with two mixers in Weaver architecture.

Since the receiver designed in this dissertation chooses the low IF architecture, the mixer implemented in this chapter is integrated with active inductor-based band pass filter to filter out high frequency carrier and reserve the IF signal. Meanwhile, the active circuits also provide the benefit of gain improvement and area efficiency.

8.2 Mixer Design

8.2.1 SIDO Mixer for Weaver Design

Weaver image rejection architecture uses two stages of mixer to demodulate the RF signal into IF band, and the first stage circuit uses SIDO design shown in Fig 8.2.1 which is a simplified version of Gilbert implementation introduced in next section.

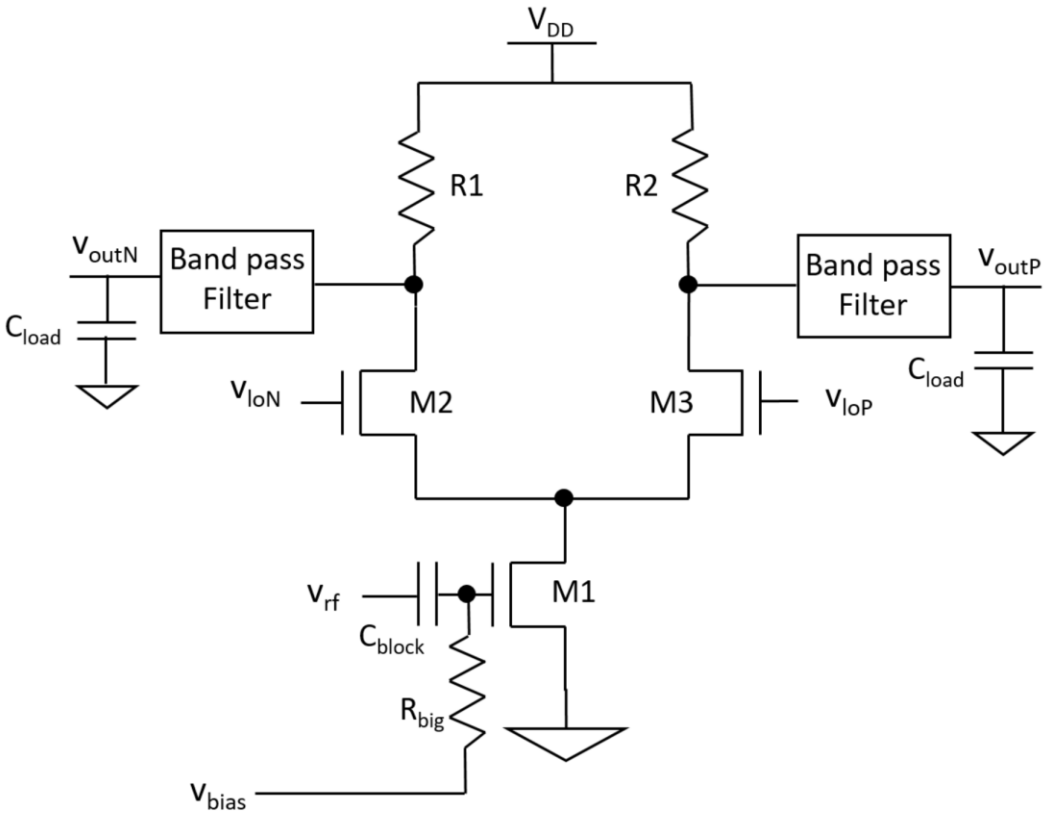

Fig 8.2.1 Schematic diagram of SIDO mixer

At this stage, signal with 5.25 GHz of targeting channel center frequency is down-converted to 750 MHz signal by SIDO mixer when local oscillator generates 4.5 GHz LO signals. Furthermore, since next stage Gilbert mixer is designed with two differential inputs, the single-input-dual-output feature of SIDO mixer can convert the input signal from previous RF stage single pin mode into differential format. The output 750 MHz signal feeds into next stage Gilbert mixer for further processing.

8.2.2 Gilbert Mixer

Fig 8.2.2 shows the schematic of Gilbert cell mixer. In order to design the mixer with reasonable power consumption, the sum of current flowing through both M1 and M8 are set to be no more than 5 mA. So, in the following calculation, both transistors passed current and gate voltage are set to 2.5 mA and 0.5 V respectively. Thus, the resistance of R3 can be calculated:

$$\frac{1.2V-0.5V}{2.5mA} = 280\Omega \tag{8.2.1}$$

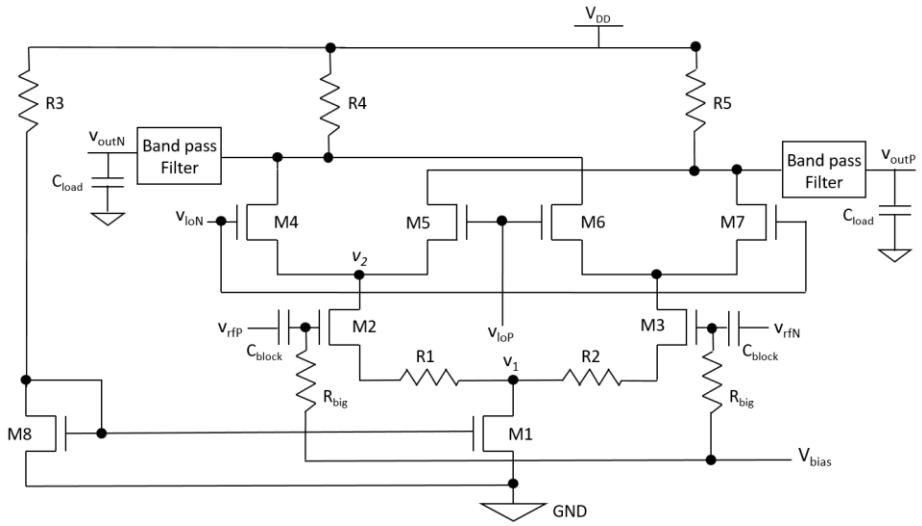

Fig 8.2.2 Schematic diagram of Gilbert Mixer

Since the trans-conductance value of transistor is proportional to circuit gain, all the transistors need to work at saturation region to have the largest trans-conductance and sufficient gain of mixer design. Apply the long channel NMOS saturation current equation used in this part:

$$I_{ds} = \frac{1}{2} K_n * \frac{W}{L} * (V_{GS} - V_{T0})^2 * (1 - \lambda V_{DS}) \quad (8.2.2)$$

In Eq 8.2.2, W and L represents the transistor width and length. Based on single NMOS transistor simulation result, at length = 400 nm condition, the transistor threshold voltage (V_{T0}) is 0.386 V, process gain (K_n) is 1.03 mA/V^2, and channel length modulation (λ_n) is 0.43 V^{-1}. For M8 transistor, substitute current limitation and gate voltage assumption to Eq 8.2.2, the total width is 123 μm by solving the equation below:

$$I_{ds8} = 2.5mA = \frac{1}{2} * 1.03mA/V^2 * \frac{W_8}{400nm} * (0.5 - 0.386)^2 * (1 - 0.43 * 0.5) \quad (8.2.3)$$

To make M1 transistor working in saturation region, V_{DS} must be greater than (V_{GS} – V_{T0}), so that v_1 in Fig 8.2.2 is set to be 0.2 V. And current flowing through M1 transistor can be calculated as:

$$I_{ds1} = 2.5mA = \frac{1}{2} * 1.03mA/V^2 * \frac{W_1}{400nm} * (0.5 - 0.386)^2 * (1 - 0.43 * 0.2) \quad (8.2.4)$$

So, the width of M1 is calculated as 137.6 μm.

The conversion gain of Gilbert cell mixer is expressed as:

$$A_v = \frac{2}{\pi} * \left(\frac{R_L}{R_S + \frac{1}{g_m}}\right) \quad (8.2.5)$$

As current passing M1 is divided in two, if M2 and M3 have the same size, and M4, M5, M6, and M7 are identical, the current flowing through R4 is 1.25 mA. Assuming the output waveform has 1.0 V offset voltage, then R4 and R5 should equal to 160 Ω. Setting R_S to be 10 Ω, then the trans-conductance of M2 and M3 can be solved using Eq 8.2.5, and the result is 10.8 mA/V. Apply trans-conductance equation to M2 transistor:

$$10.8mA/V = \sqrt{\frac{2*1.03mA/V^2*W_2*1.25mA}{400nm}} \quad (8.2.6)$$

Thus, $W_2 = W_3 = 18.1$ μm.

Apply Eq 8.2.2 to M2 and M4 transistors, then

$$1.25mA = \frac{1}{2} * \frac{1.03mA}{V^2} * \frac{18.1\mu m}{400nm}(V_{bias} - 0.2 - 0.386)^2(1 - 0.43(V_2 - 0.2)) \quad (8.2.7)$$

$$0.625mA = \frac{1}{2} * \frac{1.03mA}{V^2} * \frac{W_4}{400nm}(V_{lo} - V_2 - 0.386)^2(1 - 0.43(V_{outDC} - V_2)) \quad (8.2.8)$$

Assume V_2 = 0.4 V, V_{lo} = 1.2 V, and V_{outDC} = 1 V, then the V_{bias} and width of transistor M4 can be solved as 0.83 V and 2.25 μm, respectively.

Therefore, all the components parameters are solved to high conversion gain with reasonable power consumption. In practical design, these theoretical results may be different from real value, due to the unconsidered parasitic capacitance and resistance.

However, this IF output signal is noisy and still coupled with high frequency carrier signal, thus a band pass filter is needed to reserve only the certain frequency range mixer output signal that contains the wanted channel data and pass them to next stage for future signal extraction.

If the filter is built with traditional RLC parallel structure as shown in Fig 8.2.3, the frequency response formula of center frequency is given below:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (8.2.9)$$

In Eq 8.2.9, f_c is the center frequency and it equals to 250 MHz as required by targeting channel (channel 50 of 802.11ac). If output capacitance is set to be 100 fF, the inductance is calculated as 4053 nH. As discussed in previous chapters, large passive inductance usually means large consumption of on-chip area. Therefore, this band pass filter is implemented with active inductor in chapter 4 to minimize the circuit area usage.

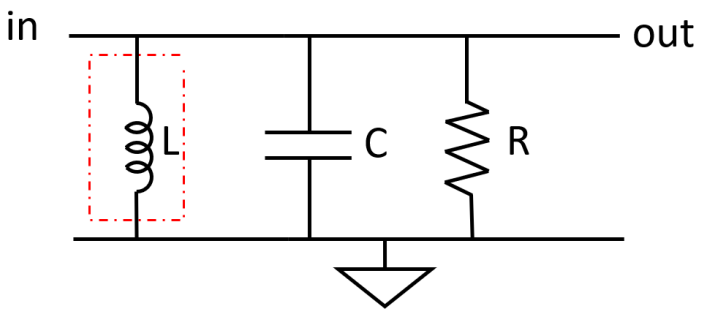

Fig 8.2.3 Conventional R-L-C band pass network

8.2.3 SIDO Mixer for Hartley Design

The SIDO mixer used in Hartley architecture is the same as the SIDO mixer employed in Weaver. By feeding the 5 GHz LO signal into the circuit, mixer is able to down-convert the wanted 5.25 GHz RF signal to 250 MHz low frequency IF signal. Attach the AIBPF designed with 250 MHz center frequency to mixer, the Hartley system perform the frequency conversion with only one stage mixer.

8.3 Simulation Results

Both SIDO and Gilbert mixers are built and simulated in Cadence software with 90 nm technology. Performance of single mixer, filter and combined system is evaluated with some key parameters in frequency conversion.

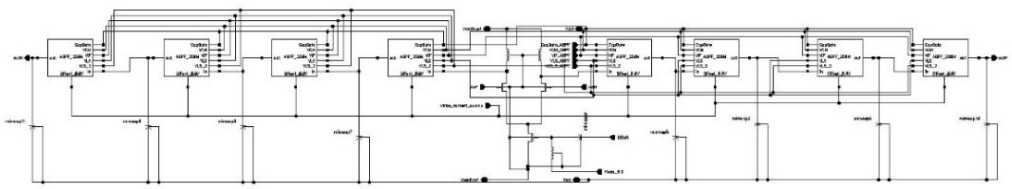

Fig 8.3.1 Schematic diagram of SIDO mixer system.

8.3.1 SIDO Mixer of Hartley and Weaver Design Simulation Results

The schematic diagram of designed SIDO mixer system is shown in Fig. 8.3.1, and the simulation results of mixer and filter are measured with system internal node to get the circuit properties with actual load. As discussed in previous section, both Weaver and Hartley employ the same SIDO mixer to perform the frequency conversion.

To make the SIDO mixer output have offset of 0.6 V, the quiescent operating point simulation is performed with V_{bias} set to be a variable as shown in Fig 8.3.2. The result indicates a 547.9 mV DC voltage is needed as bias voltage to provide 600 mV output offset of the circuit. Besides, under this bias voltage, the quiescent current flowing though mixer is 292.7 µA, which results in the total power consumption of 351.24 µW.

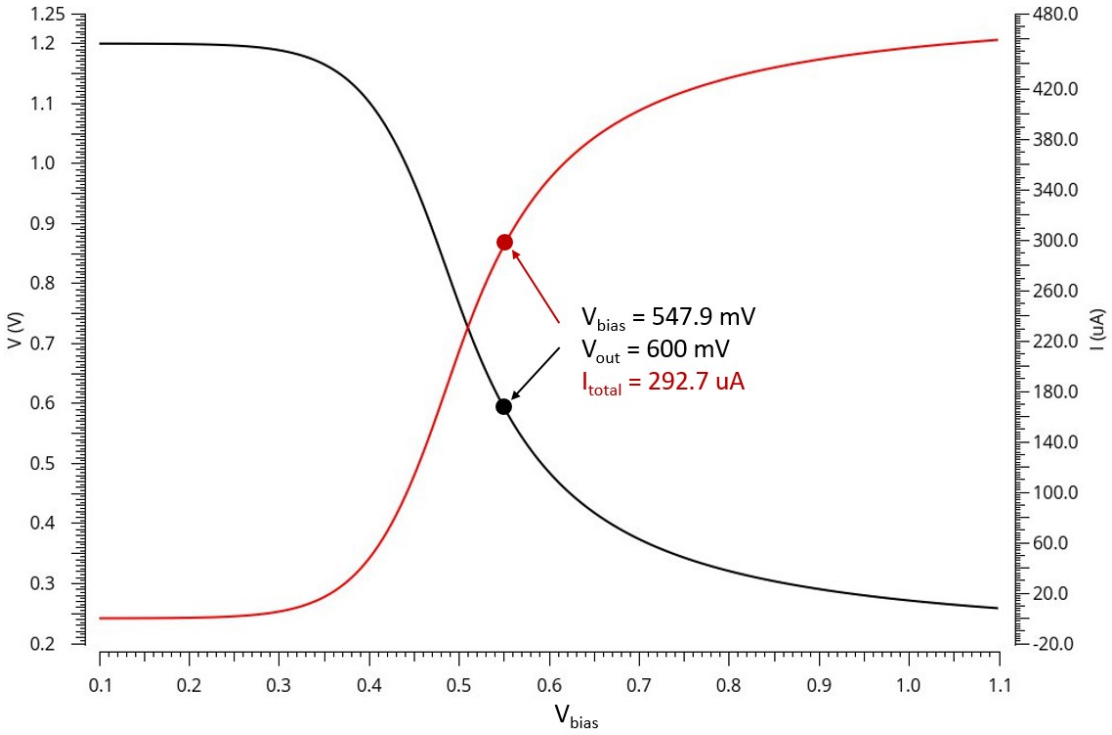

Fig 8.3.2 Quiescent simulation result of SIDO mixer

The frequency response waveform of AIBPF modified in this stage is demonstrated in Fig 8.3.3 with center frequency of 750 MHz and bandwidth of 588 MHz. In order to further improve the gain and bandwidth performance, there are 4 AIBPFs connected in series to form the filter stage. The result in Fig 8.3.4 indicates that this multi-stages AIBPF provides gain of 18.292 dB and bandwidth of 255 MHz. Therefore, all signal within channel 50 is down-converted to lower frequency region and pass to next stage Gilbert mixer.

The time domain transient analysis simulation result is shown in Fig 8.3.5 with 5.25 GHz frequency and 10 mV amplitude input sine wave. The 750 MHz output waveform has 119.3 mV amplitude and the linear gain calculated by transient analysis result is 11.93.

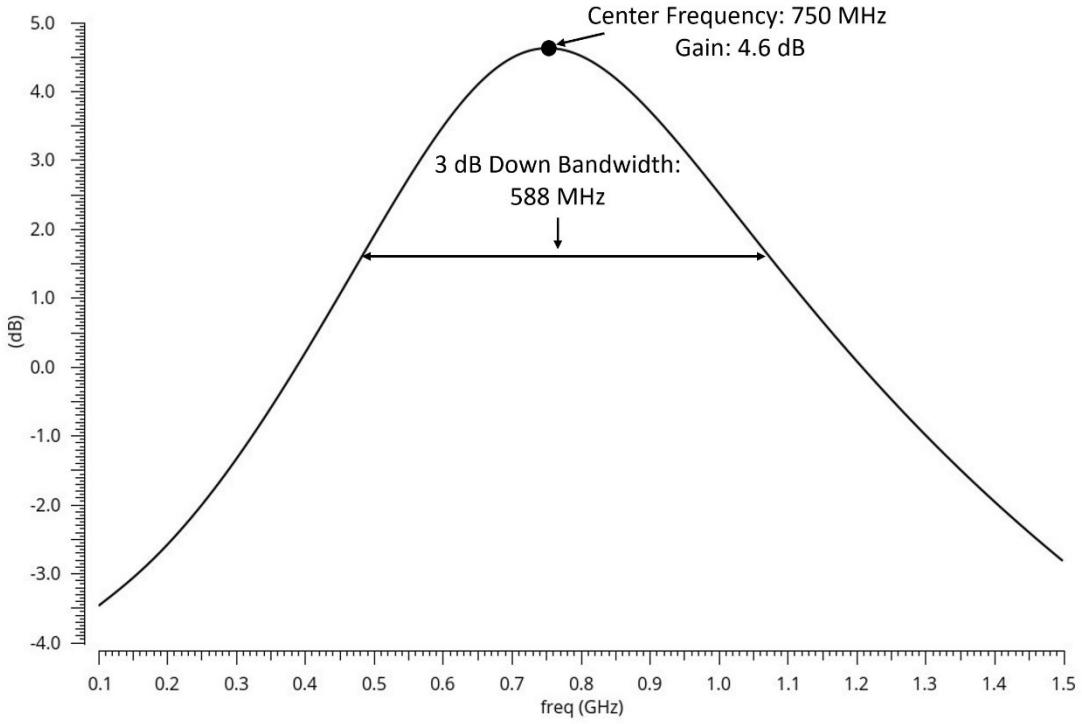

Fig 8.3.3 Frequency response simulation result of AIBPF modified for SIDO mixer

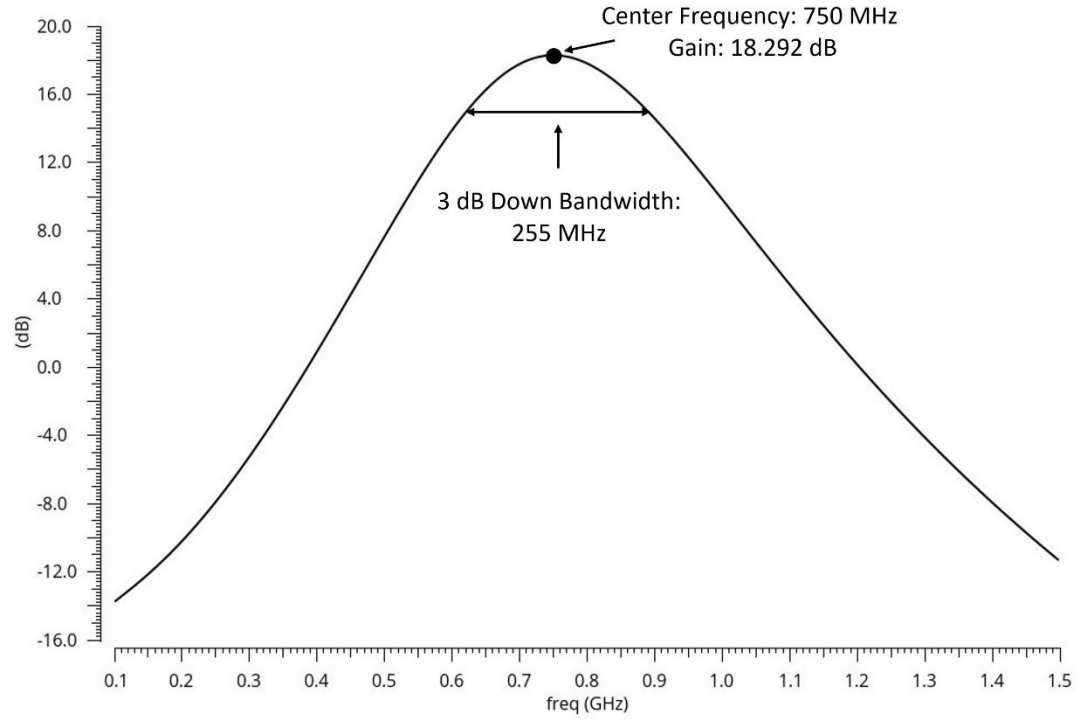

Fig 8.3.4 Frequency response simulation result of 4 stages AIBPF in series in Weaver design.

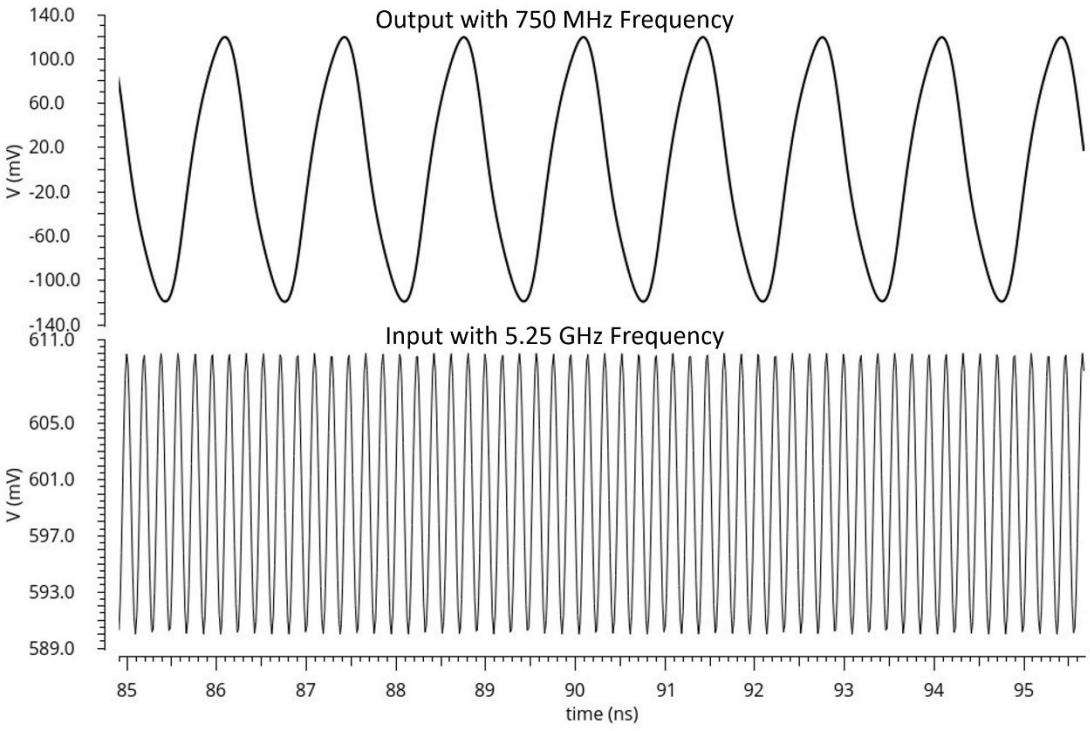

Fig 8.3.5 Time domain transient analysis result of SIDO mixer with AIBPF in Weaver design

The Fig 8.3.6 contains the noise performance of the first stage frequency down-conversion system (SIDO mixer plus AIBPFs). As shown in simulation result, the noise figure of this stage is 23.7 dB at converted signal center frequency of 750 MHz. Even though, this number is a little higher than some of the mixer design in literature, considering multiple active circuits is built in this stage and provide large gain, this NF value is acceptable. Besides, with the low noise and large gain design of previous amplifier stages, the noise performance of mixer stage does not show large impact on entire receiver system noise parameter. Furthermore, the large gain feature of the SIDO mixer based first frequency conversion stage can mitigate the noise effect of second Gilbert mixer stage.

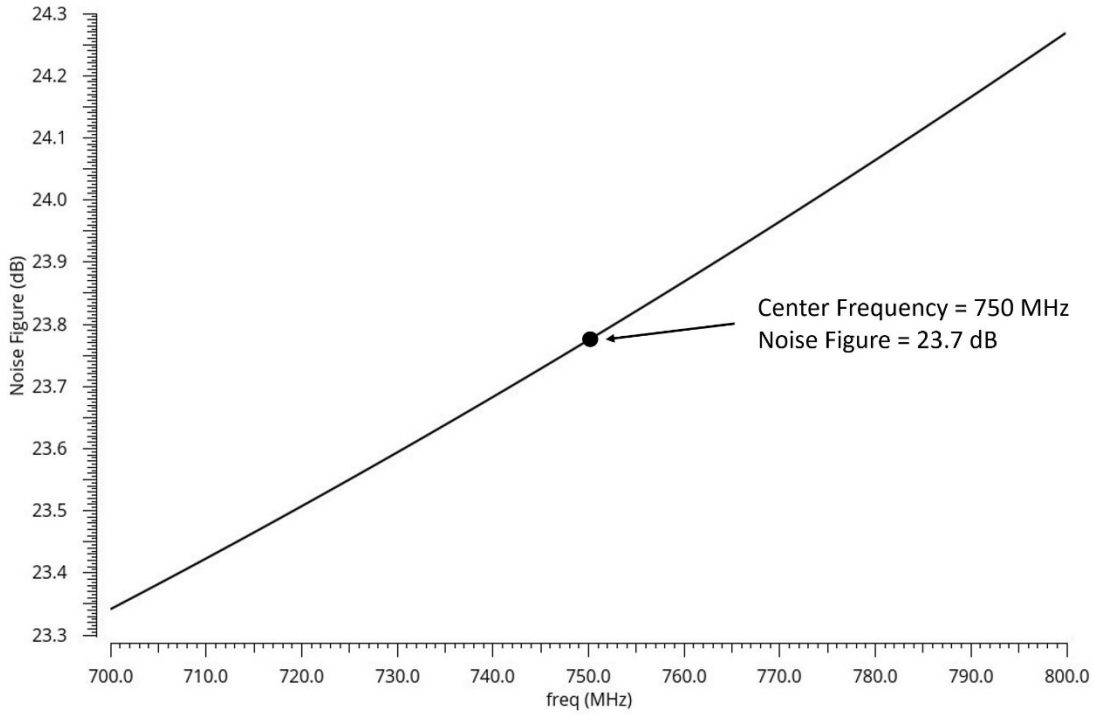

Fig 8.3.6 Noise figure simulation result of first stage frequency conversion system consisted by SIDO mixer and AIBPFs in Weaver design

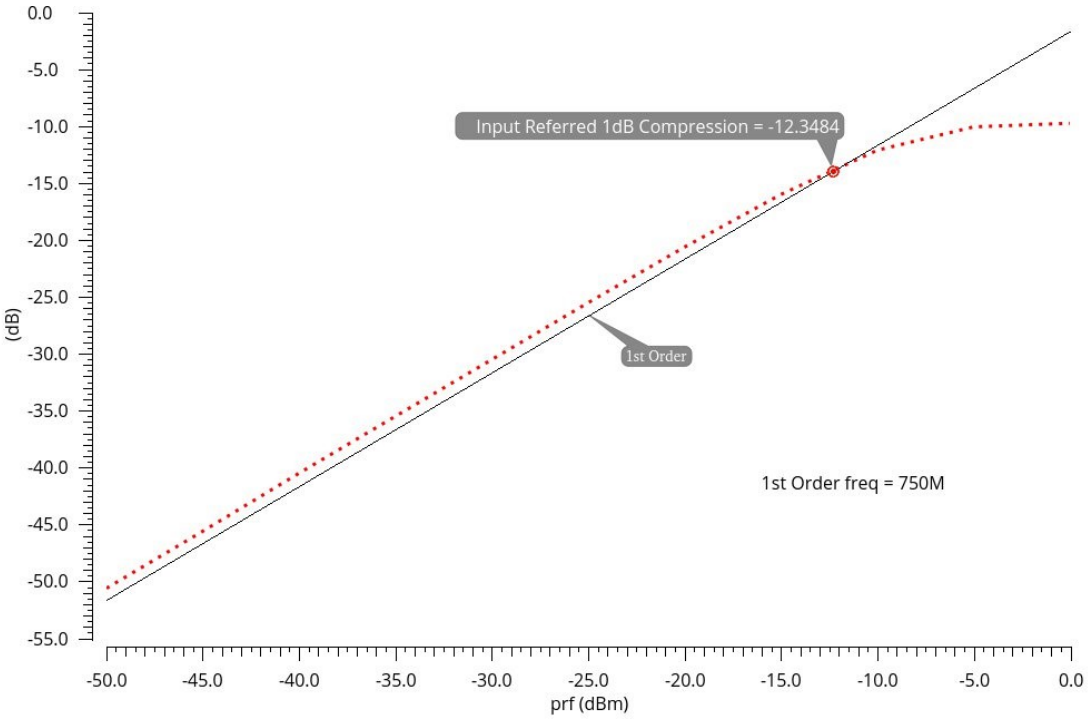

Fig 8.3.7 1dB compression simulation result of SIDO mixer in Weaver design

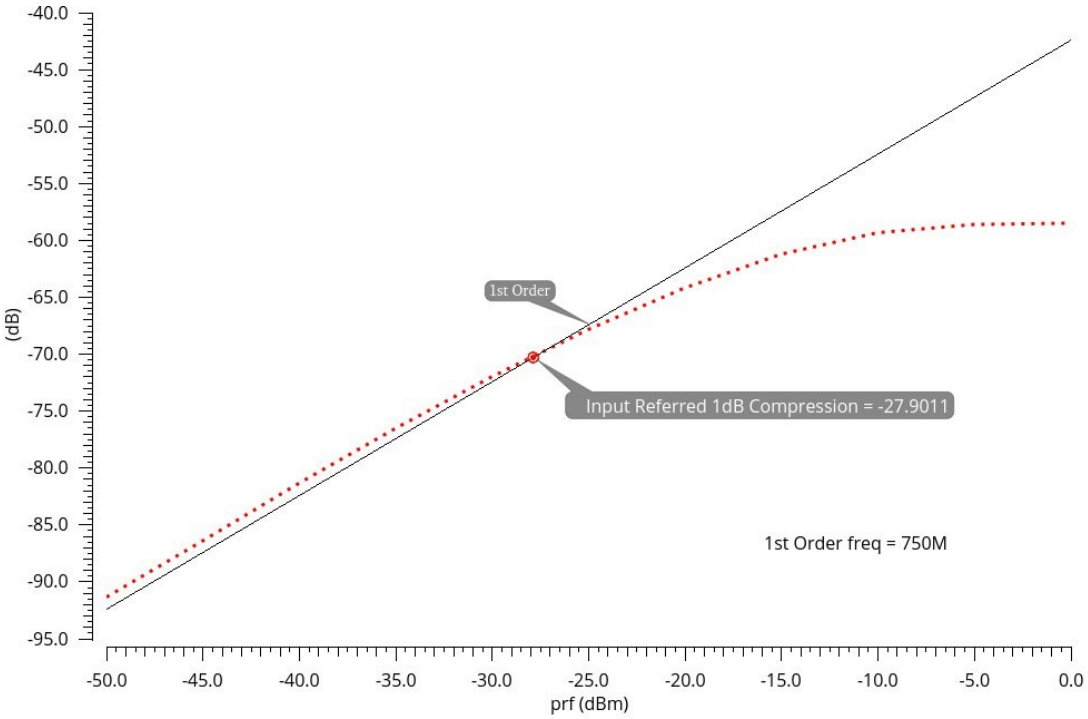

Fig 8.3.8 1dB compression simulation result of SIDO mixer connected with AIBPFs in Weaver design

Fig 8.3.7 and 8.3.8 demonstrate 1 dB compression point of SIDO mixer and entire frequency conversion system including SIDO mixer and AIBPFs, respectively. For SIDO mixer, the compression point is -12.35 dBm. If the design is integrated with AIBPF, then the compression point drops to -27.9 dBm. It can be seen from these two graphs that the tradeoff of adding extra gain to the system is the degradation of linearity.

The IIP3 simulation result of SIDO mixer is -4 dBm which can be found in Fig 8.3.9 with down-converted third order signal of 749 MHz. Under the same testing setup, the IIP3 result of SIDO mixer plus AIBPFs is -24.82 dBm shown in Fig 8.3.10.

To evaluate the capability of designed SIDO mixer suppressing the supply power variation to its output, the Power Supply Rejection (PSR) simulation is performed. The smaller value of this result indicates the system is less sensitive to the variation. As shown in Fig 8.3.11, the SIDO mixer has PSR value of -125 dB at frequency of 750 MHz.

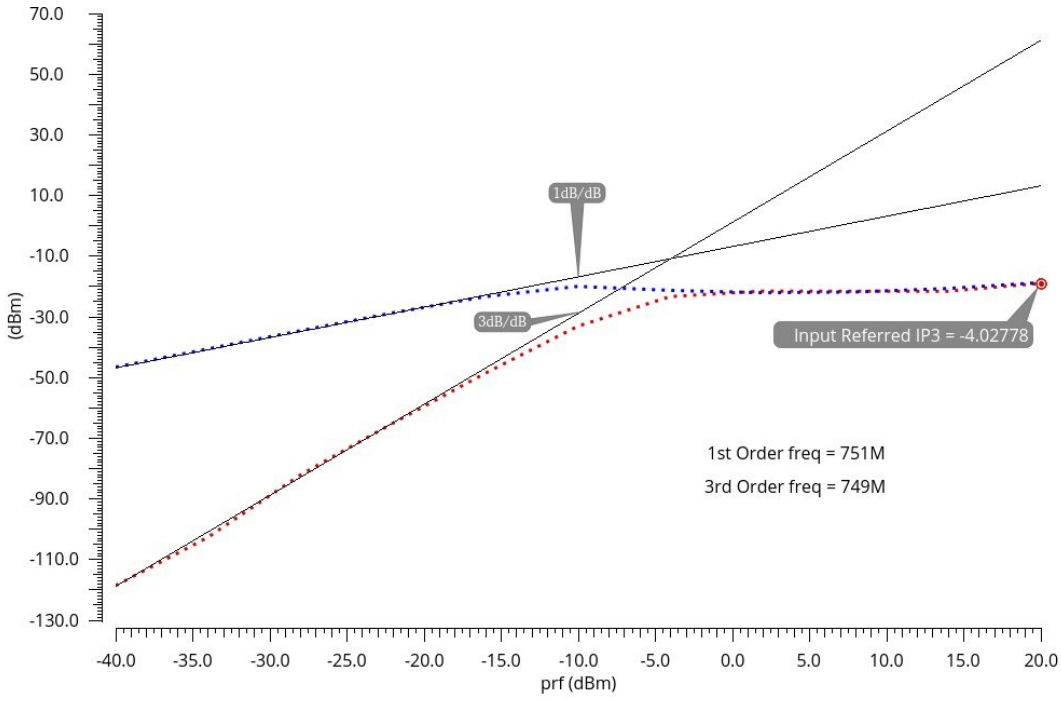

Fig 8.3.9 1dB compression point of SIDO mixer in Weaver design

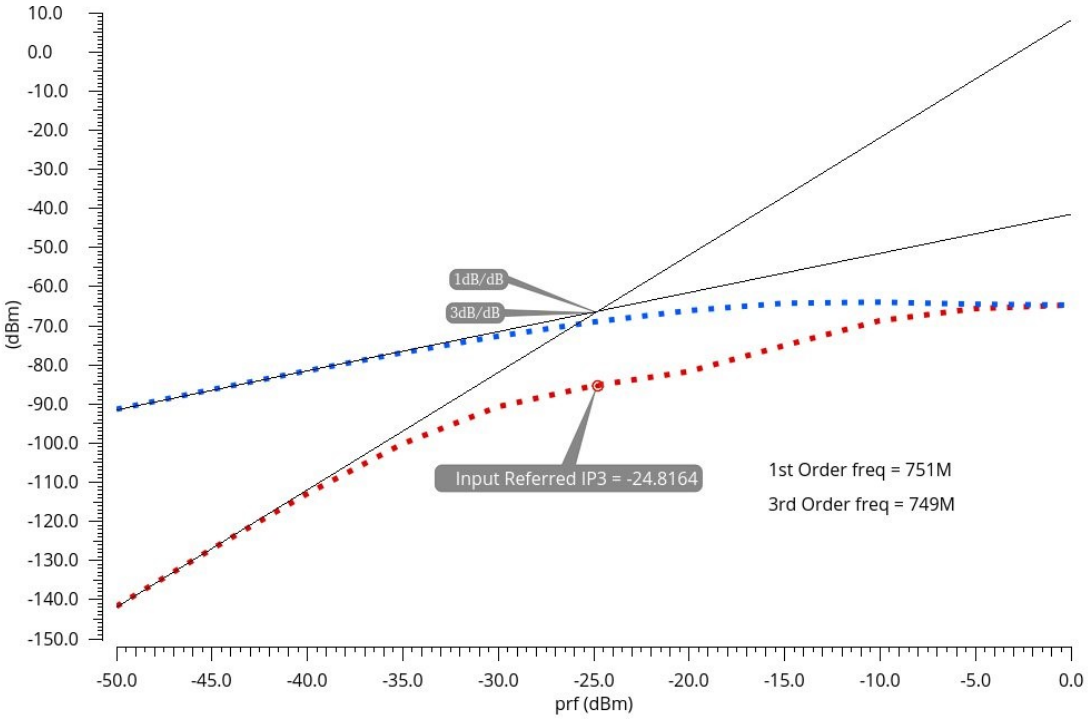

Fig 8.3.10 IIP3 simulation result of SIDO mixer plus AIBPFs in Weaver design

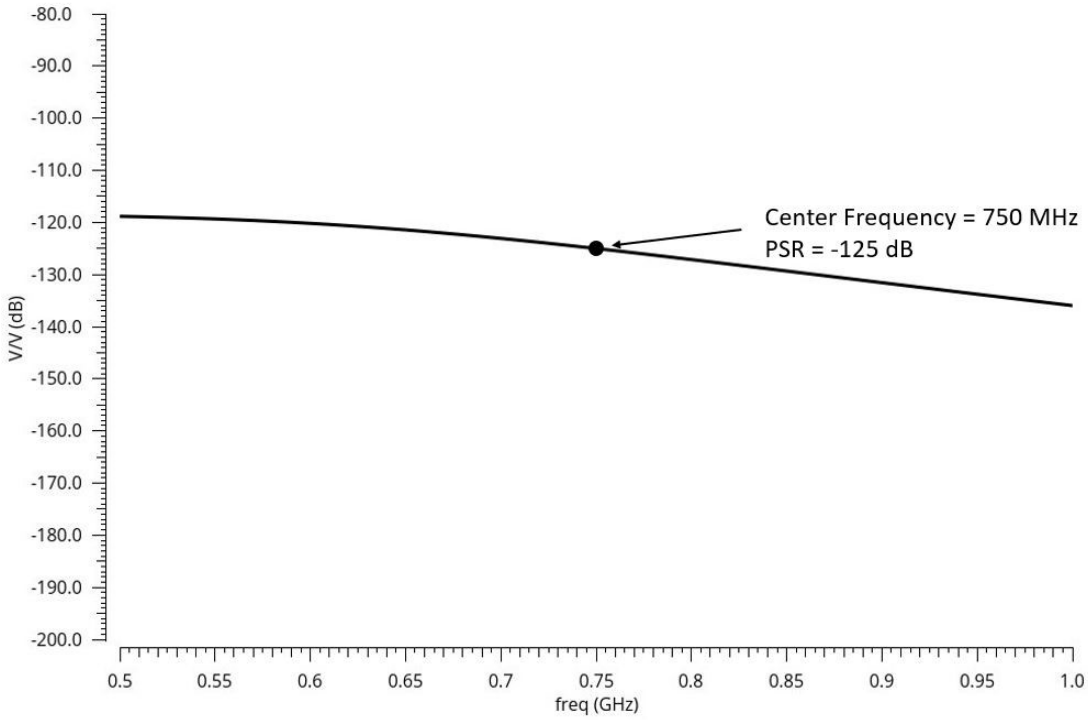

Fig 8.3.11 Power supply rejection simulation result of SIDO mixer in Weaver design

The SIDO mixer designed for Hartley system has the same architecture with transistor size and control voltages properly adjusted. The simulation results are listed in Table 8.3.1.

Table 8.3.1 Simulation Result of SIDO Mixer Designed for Hartley System

Parameters	Value
Center Frequency	250 MHz
1 Stage AIBPF Gain	11.7 dB
4 Stages AIBPF Gain	48.16 dB
1 Stage AIBPF 3 dB Bandwidth	385.27 MHz
4 Stages AIBPF 3 dB Bandwidth	156.91 MHz
SIDO + AIBPF Noise Figure	21.85 dB
SIDO + AIBPF 1 dB Compression Point	-39.17 dBm
SIDO + AIBPF IIP3	-34.07 dBm
PSR	-137.82 dB

8.3.2 Gilbert Mixer of Weaver Design Simulation Results

The schematic diagram of designed Gilbert mixer system is presented in Fig. 8.3.12, and the simulation results of mixer and filter are measured with system internal node to get the circuit properties with actual load.

The quiescent operating point simulation result of Gilbert mixer is shown in Fig 8.3.13 with bias voltage of 596.9 mV and current of 800 μA when output DC voltage equals to 1 V. The power consumption of designed Gilbert mixer is 960.12 μW.

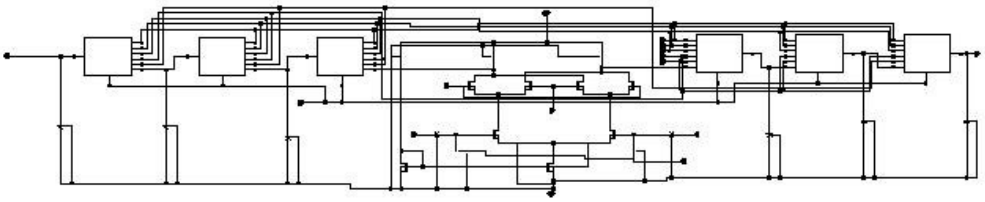

Fig 8.3.12 Schematic diagram of Gilbert mixer.

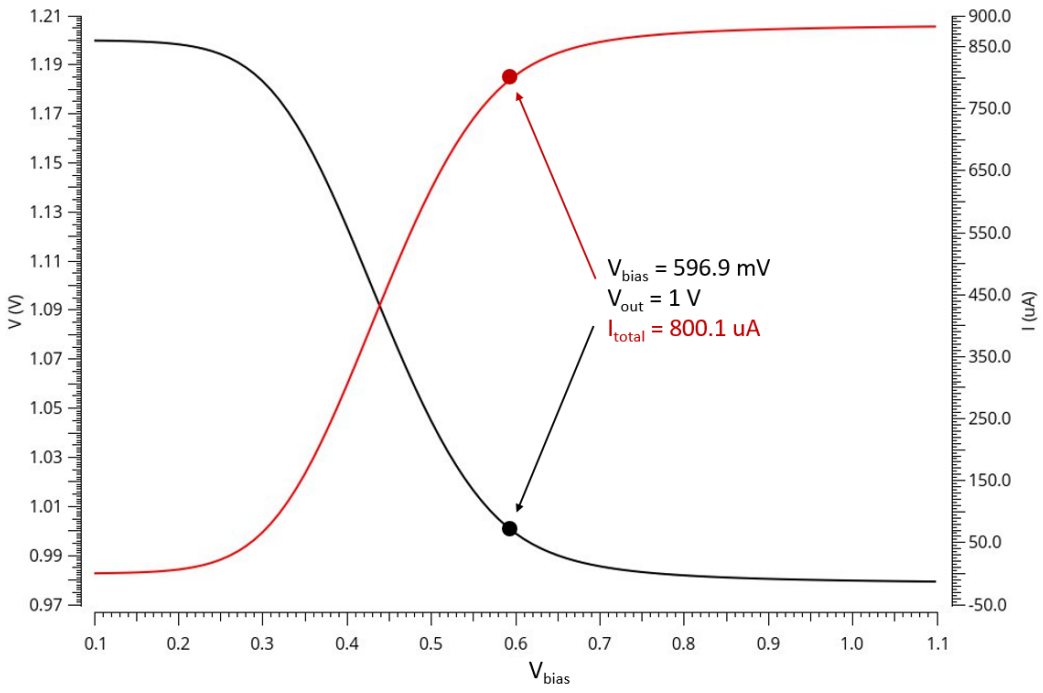

Fig 8.3.13 Quiescent simulation results of Gilbert mixer.

Fig 8.3.14 contains the frequency response waveform of AIBPF modified for this stage mixer with center frequency of 250 MHz with gain of 11.514 dB and bandwidth of 160 MHz. There are 3 AIBPFs connected in series building the band pass filter block for each mixer output node, and the overall performance is shown in Fig 8.3.15 with center frequency still locating at 250 MHz but higher gain of 36.56 dB and narrow bandwidth of 77.45 MHz. With this filter stage, the 250 MHz mixer output signal is extracted and ready to be processed by following circuit blocks.

The time domain waveform in Fig 8.3.16 indicates the mixer and AIBPFs provide gain of 14.87 dB totally when both differential inputs amplitude is 20 mV.

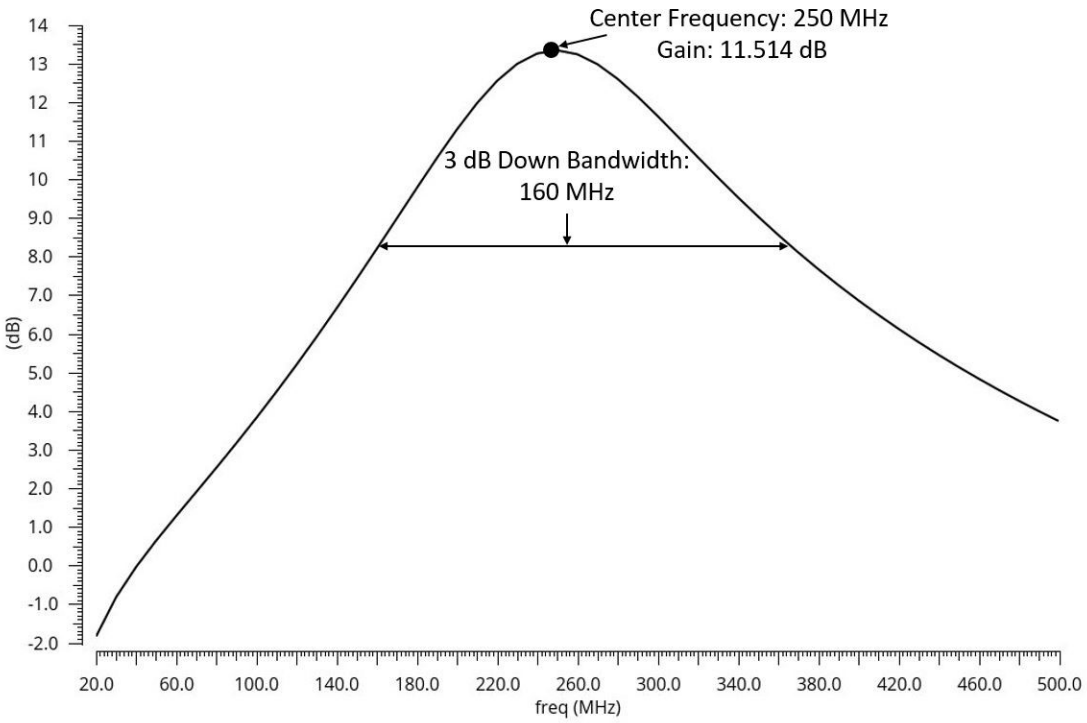

Fig 8.3.14 Frequency response simulation result of AIBPF modified for Gilbert mixer

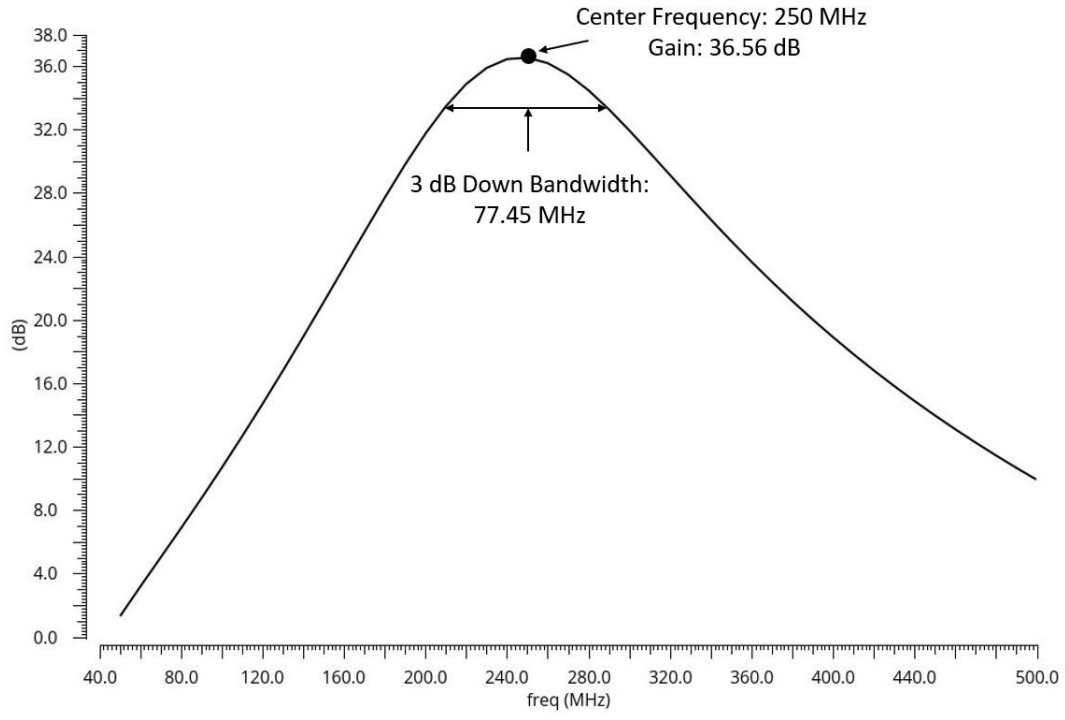

Fig 8.3.15 Frequency response simulation result of 3 stages AIBPF in series.

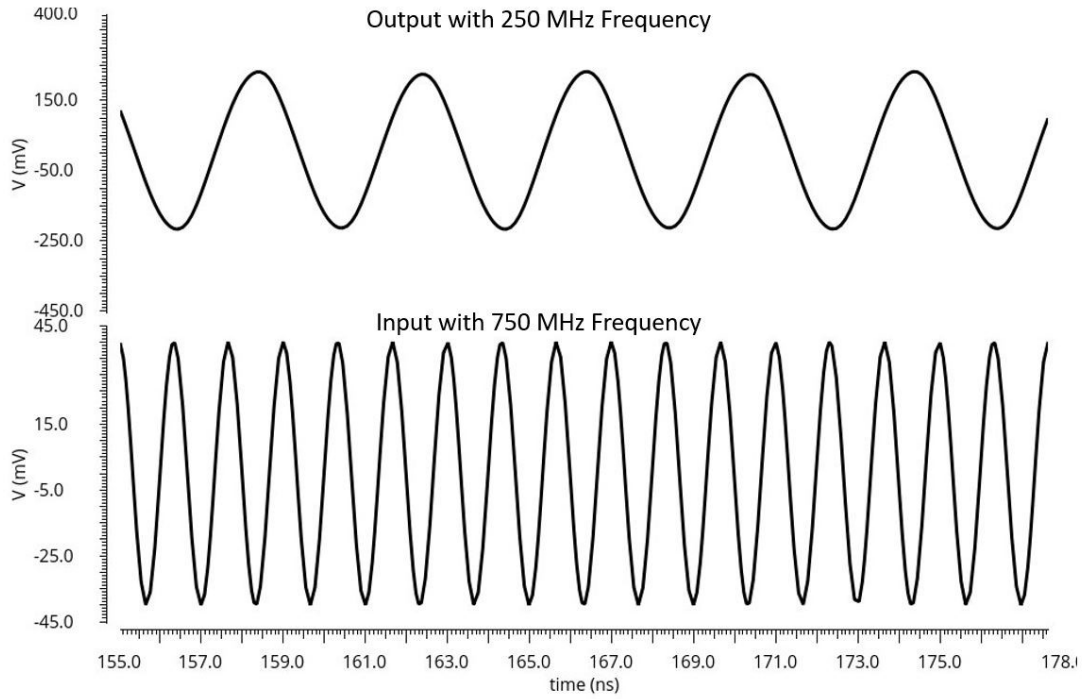

Fig 8.3.16 Time domain simulation result of Gilbert mixer with AIBPFs

The drawback of Gilbert mixer circuit is the poor noise figure value. Combining both mixer and AIBPFs, the simulation results in Fig 8.3.17 indicates noise figure of 76.25 dB at center frequency of 250 MHz.

1 dB compression point simulation results of Gilbert mixer and entire frequency conversion stage with AIBPFs attached on mixer are shown in Fig 8.3.18 and 8.3.19, respectively. By adding the AIBPFs to filter out noise and increase gain, the 1 dB compression point decreases from -1.84 dBm to -14.76 dBm.

Fig 8.3.20 and 8.3.21 contains the IIP3 simulation results of Gilbert mixer and entire frequency conversion stage with AIBPFs attached on mixer, respectively. As shown on graphs, the Gilbert mixer has IIP3 value of -10.27 dBm and then drops to -17.48 dBm when connect the AIBPFs to it.

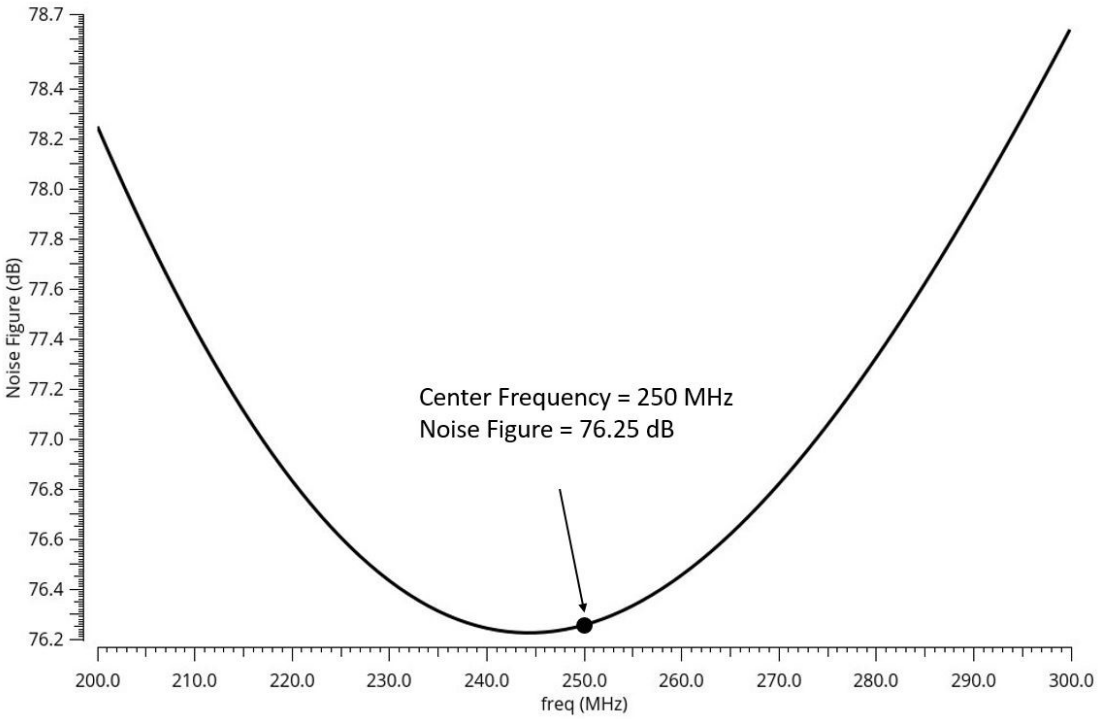

Fig 8.3.17 Noise Figure simulation result of second stage frequency conversion system (Gilbert mixer plus AIBPFs)

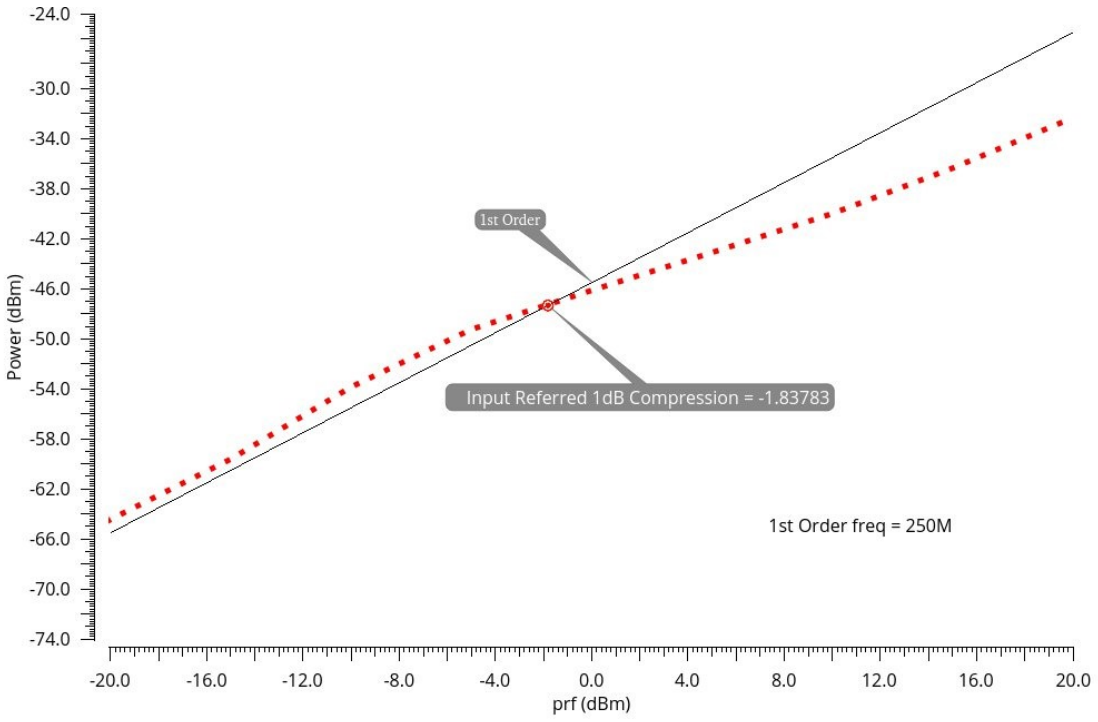

Fig 8.3.18 1 dB compression point simulation result of Gilbert mixer

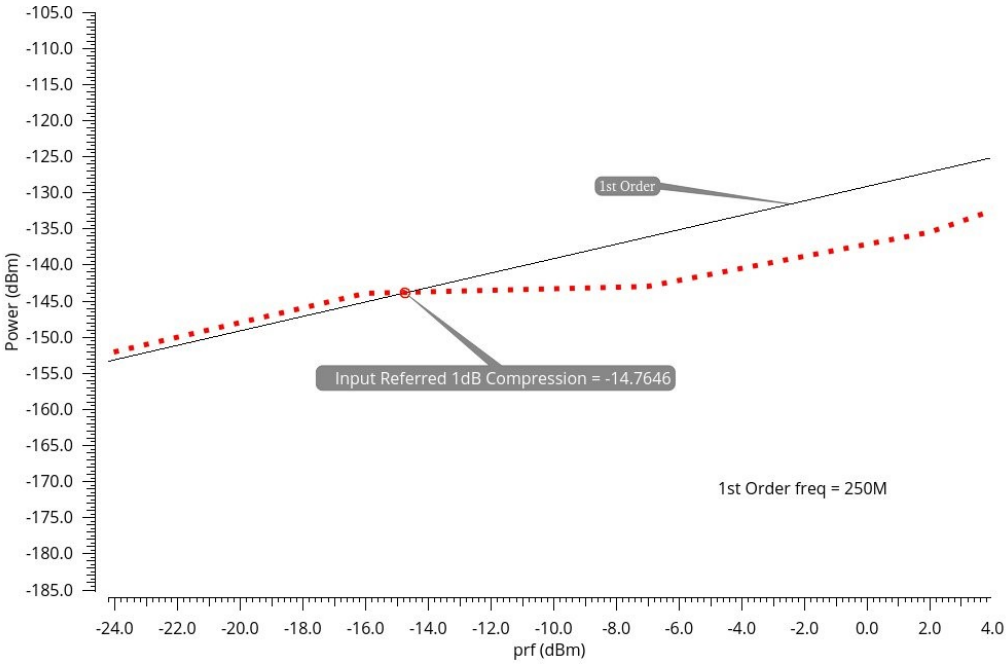

Fig 8.3.19 1 dB compression point simulation result of Gilbert mixer with AIBPFs

The supply power rejection simulation result of Gilbert mixer is shown in Fig 8.3.22 and it equals to -179.92 dB at frequency of 250 MHz.

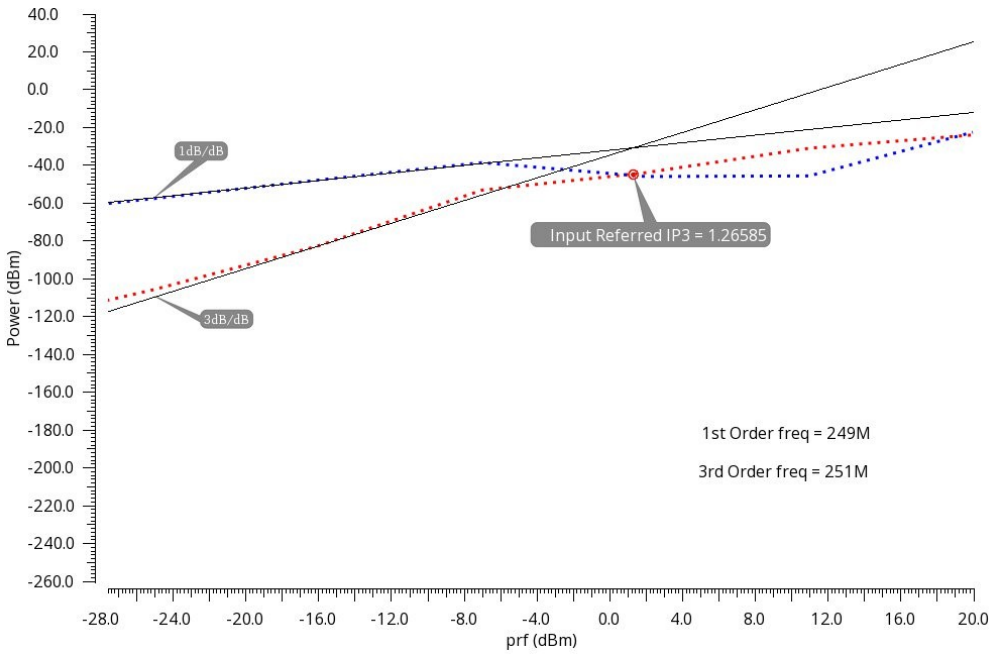

Fig 8.3.20 IIP3 simulation result of Gilbert mixer

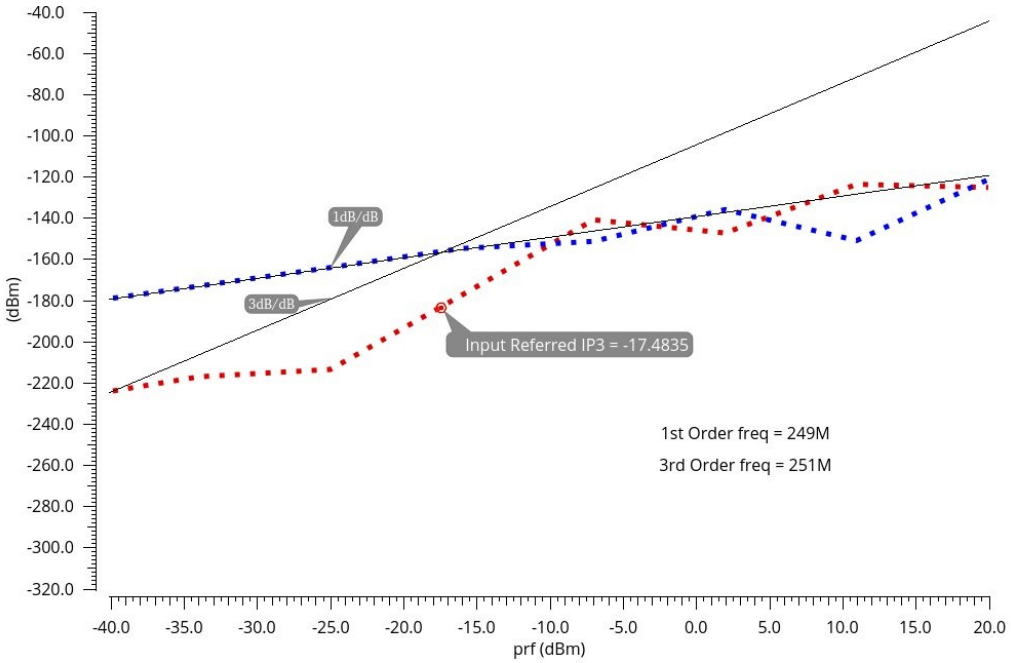

Fig 8.3.21 IIP3 simulation result of Gilbert mixer plus AIBPFs

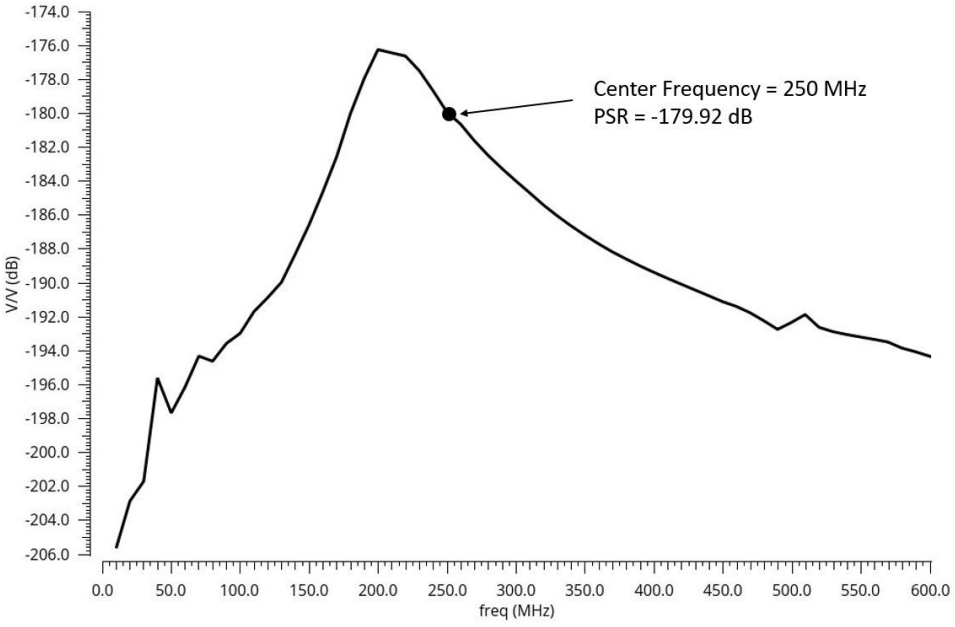

Fig 8.3.22 Power supply rejection simulation result of Gilbert mixer

8.4 Conclusion

In this section, the SIDO and Gilbert mixers are designed for building Hartley and Weaver frequency down-converting system. The AIBPFs are optimized to pass the targeting low frequency IF signal and filter out the high frequency noise. Both mixers provide large gain and good quality factor by taking the advantage of active filter. The SIDO mixer has better noise performance and less power consumption, while the Gilbert design offers better supply power rejection. The system performance of Hartley and Weaver design are introduced along with entire receiver chain simulation results in the future chapters.

IX. Phase Locked Loop

9.1 Introduction

Phase Locked Loop (PLL) circuit is widely used in modern transceiver design to provide many of system signals, such as carrier, clock, etc. In WLAN communication technique, the low frequency data at transmitter section is modulated on a high frequency carrier signal before transmitting. Such carrier signal is removed at receiver section by mixer circuitry to recover the transmitting information for following data processing. The PLL circuit built in WLAN system is employed to generates high frequency carrier signal which is also called Local Oscillator (LO) signal in both transmitter and receiver paths. In order to satisfy system specifications, the PLL must deliver high stability, short settle time, and low phase noise with reasonable power consumption [28].

As discussed in previous chapters, the receiver design in this dissertation needs quadrature 5GHz LO signals to down-convert RF signal into IF band and perform image rejection with Hartley architecture. Therefore, in this chapter, a quadrature outputs Voltage-Controlled Oscillator (VCO) resonating at 5GHz is introduced along with feedback control structure PLL system to meet the receiver specifications.

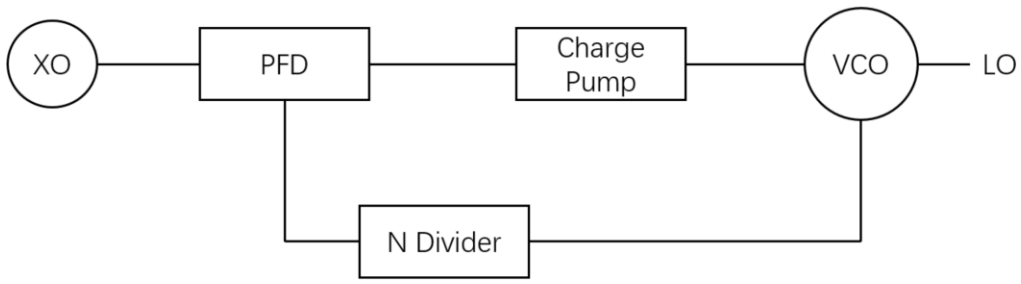

Fig 9.2.1 System overview of proposed PLL design

9.2 System Topology and Sub-Circuit Introduction

A feedback control structure PLL is consisted of Crystal Oscillator (XO), Phase Frequency Detector (PFD), charge pump, VCO and N divider as shown in Fig 9.2.1. Signal from VCO output feeds back to PFD with 1/N original frequency through N divider to compare the phase and frequency with XO reference signal. If any frequency variation of VCO is detected, the PFD generates a signal to indicate the variation and control charge pump adjusting VCO bias voltage until the frequency variation is eliminated.

9.2.1 Phase Frequency Detector

In order to recognize the frequency of phase difference between reference signal and feedback VCO output, the PFD compares the time of each signal rising edge and generates the corresponding digital signal to indicate such variation. Conventionally, two D Flip Flop (DFF) plus a reset AND gate can form a PFD system as shown in Fig 9.2.2. This design provides wide phase difference detection range from -2π to 2π which ensure the entire PLL system having short response time and good stability [28]. The operation of this PFD can be described as: 1) At initial state, Ref and VCO are equal to '0', and two DFF output (Q1 and Q2) are also equal to '0'. Therefore, the output of AND gate is 0 and two DFFs are not reset; 2) If the rising edge of Ref arriving at DFF is earlier than VCO, then Q1 rises to '1' and Q2 remains at '0'. 3) When VCO rising edge arrives DFF2, Q2 becomes '1', which makes the output of AND gate rise to '1' and reset both DFF outputs to '0'; 4) System returns to initial state and waits the rising edge of next signals.

However, the drawback of this implementation is the dead zone issue which caused by small phase error between two input signals. In this case, the PFD fail to

output the correct signal as the time delay created by signal phase difference is less than the AND gate delay. So, to avoid the dead zone effect, the feedback portion of PFD design needs to be removed, and such circuit structure is used in this dissertation as shown in Fig 9.2.3 [51].

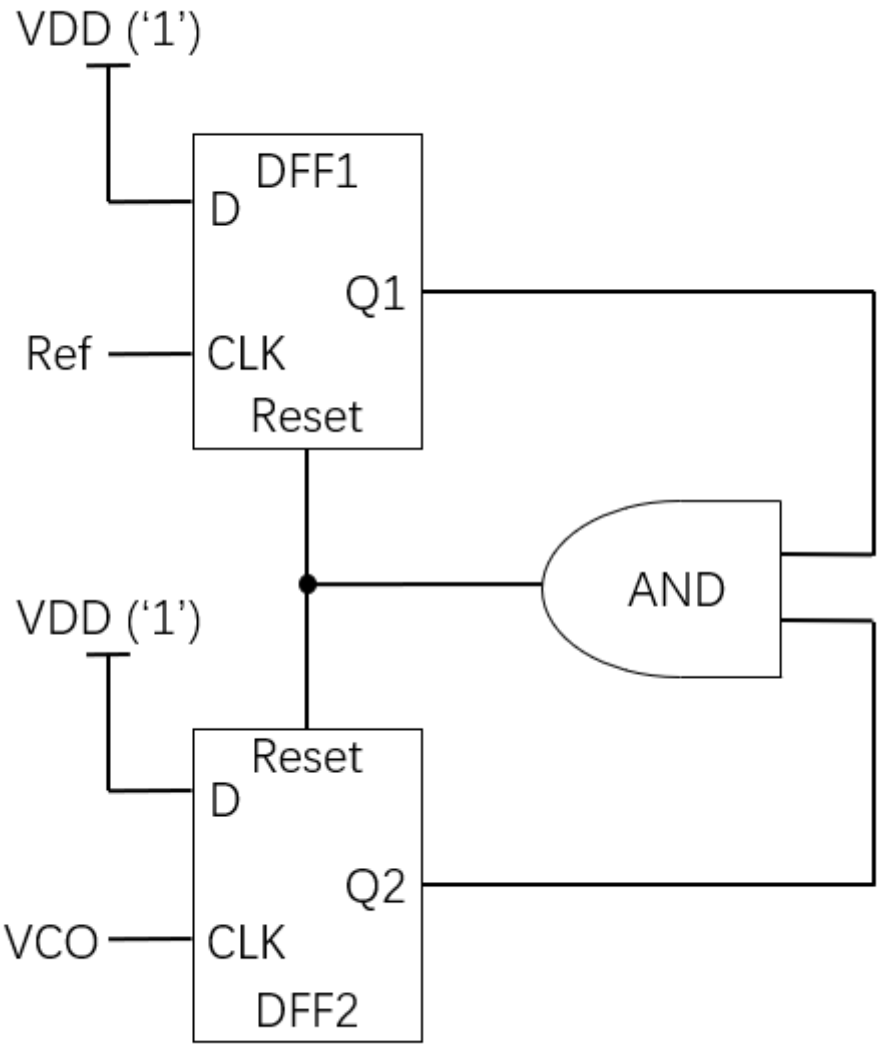

Fig 9.2.2 PFD using DFF circuit

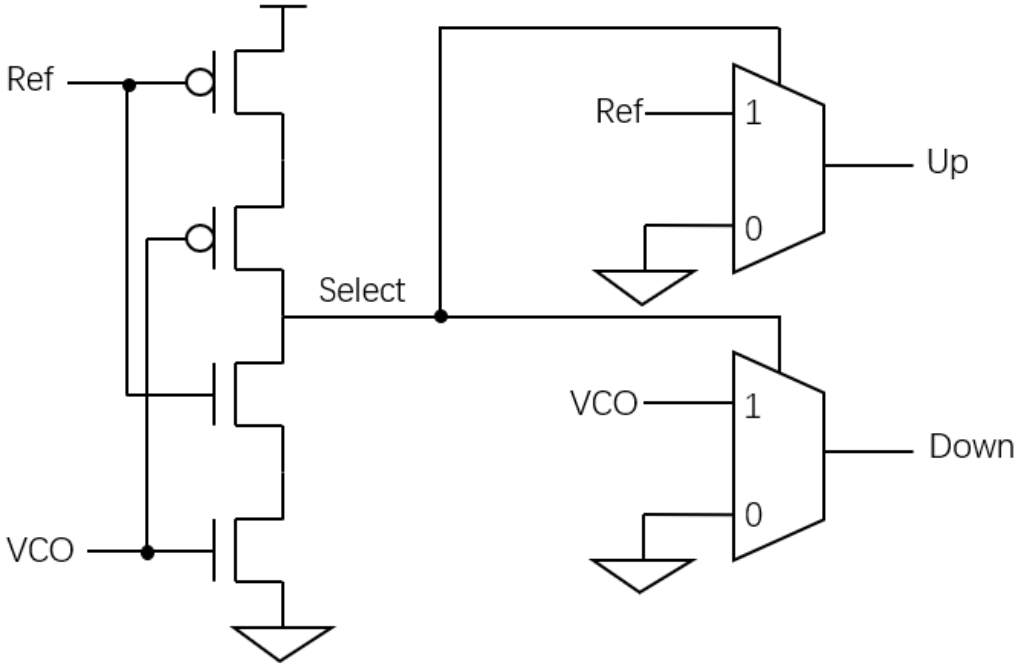

Fig 9.2.3 Proposed PFD with zero dead zone

The proposed PFD circuitry is a two-stage architecture, and the first stage output is the selection signal of second stage 2 multiplexers. At initial state, both Ref and VCO are '0', and Select is equal to 1. The second stage multiplexers output the value at input node '1', and both are '0'. If rising edge of Ref signal reaches PFD earlier than VCO, Select remain at '1', and only Up rises to '1'. When the rising edge of VCO arrives at PFD after certain delay, the Select signal is pulled down to 0, and both multiplexers output the value at input node '0' which is GND ('0'). Thus, the PFD finishes one comparison period and every node is back to initial state.

9.2.2 VCO with Quadrature Outputs

Generally, there are two types of VCO design that are popular in PLL system implementation, one is using LC tank, and another one is using delay cell to build ring

oscillator. The LC tank based architecture oscillates at passive component resonating frequency and the tuning feature is usually achieved by controlling the varactor value. Even though, the LC tank oscillator provides less phase noise, this circuitry suffers lacking wide tuning range and relatively large on-chip area due to the inductor. Therefore, in this dissertation, the proposed VCO uses ring oscillator structure to be area efficiency. Such VCO needs to have low phase noise and wide tuning range along with quadrature output characteristic.

To reach those specifications, the delay cell introduced in [50] is employed in this paper, and the schematic is shown in Fig 9.2.4. Such delay cell is consisted of differential oscillator and CMOS latch to improve the driving ability and phase noise performance.

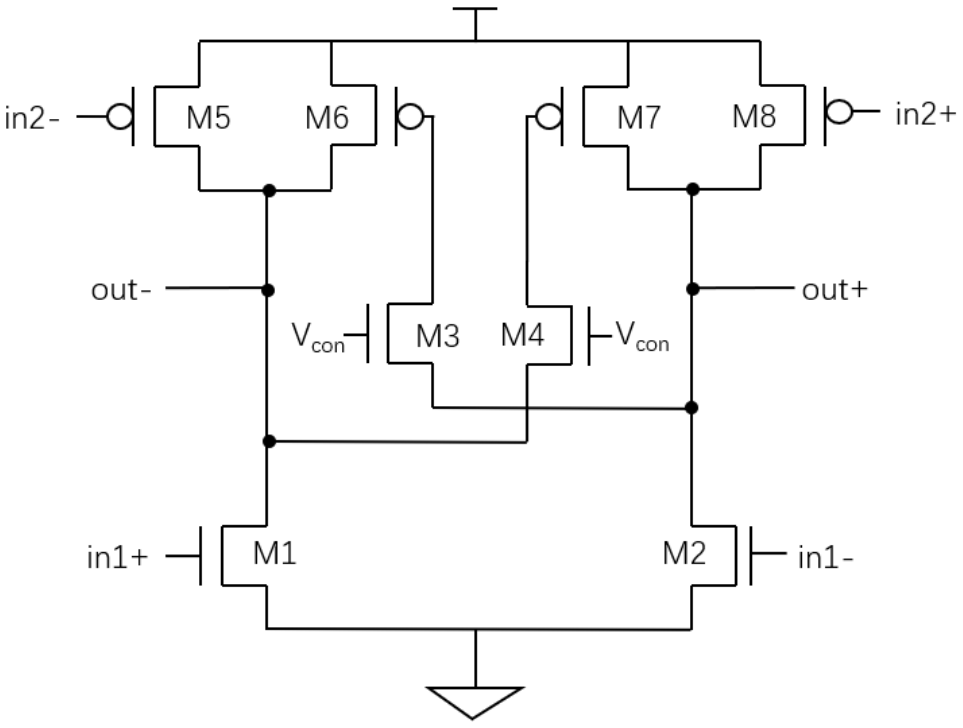

Fig 9.2.4 Schematic of proposed delay cell using in VCO

The tunability of output frequency is achieved by varying the V_{con} in Fig 9.2.4. When M3 and M4 working in linear region, the current flowing through transistor can be expressed as:

$$i_{ds2} = \mu_n * C_{ox} * \frac{W}{L} * \left[(V_{con} - V_{out} - V_{Tn})V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (9.2.1)$$

Where μ_n is the electron mobility in the channel and C_{ox} represents gate capacitance in unit area. W and L are the width and length of transistor, respectively. V_{Tn} is the threshold voltage of NMOS transistor and V_{ds} is the drain to source voltage across transistor. Thus, the equivalent resistance R of M3 and M4 are equal to:

$$R = \frac{\partial V_{ds}}{\partial i_{ds}} = \frac{1}{\mu_n * C_{ox} * \frac{W}{L} * \left[(V_{con} - V_{out} - V_{Tn}) - \frac{V_{ds}}{2}\right]} \quad (9.2.2)$$

From Eq 9.2.2, with the increment of V_{con}, the R decreases. If the parasitic capacitance is unchanged within the path from M6 and M7 to out+ and out-, the smaller value of R increases the time constant of changing M6 and M7 gate voltage and decreases the output frequency due to the stronger latch impact [50].

Fig 9.2.5 contains the VCO architecture using proposed delay cell, and it provide quadrature phase outputs with buffer connected to enhance the driving and isolation ability.

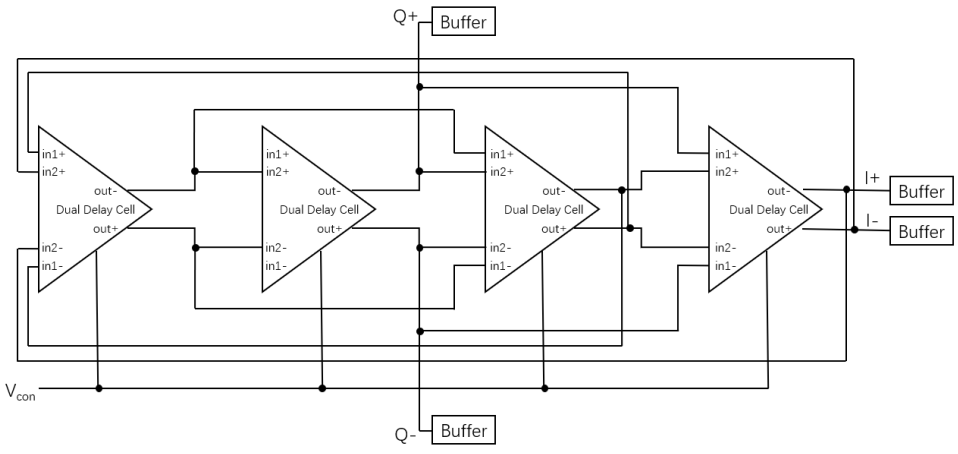

Fig 9.2.5 Schematic of quadrature outputs VCO using propose delay cell

9.2.3 Charge Pump and Loop Filter

Charge pump converts the output signal of PFD to analog voltage changing and tune the frequency of VCO. In the proposed PLL system, charge pump design uses the same circuitry as introduced in section 7.3 of chapter VII, which can pull up or pull down the control voltage of VCO based on the Up of Down pulse generated from PFD.

In order to stabilize the output of charge pump, a loop filter is an essential component to smooth the control voltage of VCO [28], and it should be placed between charge pump and VCO. A widely used design of loop filter is employing passive resistor and capacitors to provide the low pass feature and additional pole as shown in Fig 9.2.6.

To calculate the value of each component in Fig 9.2.6, and gain the flattest frequency response curve, the damping factor ξ of loop filter needs to be $\sqrt{2}/2$ as shown below [50]:

$$\xi = \frac{\omega_0}{2} * R_Z * C_Z \tag{9.2.3}$$

Where ω_0 is the bandwidth of entire loop, and it is equal to:

$$\omega_0 = \sqrt{\frac{I_{ch}}{2\pi C_Z N} K_{VCO}} \tag{9.2.4}$$

In Eq 9.2.4, I_{ch} is the charging current of charge pump and the value measured from the design in section 7.3 is 5.5 μA. C_Z is set to be 10 pF and N is the value of divider stage which is 128 in proposed PLL. K_{VCO} represent the gain of VCO (Hz/V) which can be found with simulation result, and the recommended resistance of loop filter is calculated in next section.

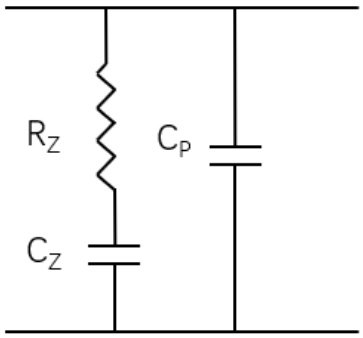

Fig 9.2.6 Loop filter with additional pole

9.2.4 N-Divider Block

To reduce the system consumption and decrease system complexity, the feedback signal from output of VCO need to pass a frequency division circuit block to lower its frequency before entering PFD. In this dissertation, the N value is set to be 128 and this number is achieved by 7 stages of divide-by-2 circuitry shown in in Fig 9.2.7. This divider features single phase clock flip-flop structure which is compatible with low power (no static power consumption), area efficiency and high frequency application.

As illustrated in Fig 9.2.8, when circuit is in initial state, both CLK and out node are equal to ‘0’. Internal node X and Y are equal to ‘1’, and out is ‘0’. In next step, feedback gets ‘0’ from previous state out node and CLK rises to ‘1’, which maintains the ‘1’ at X node and pulls down Y to ‘0’. At this state, the out is equals to ‘1’. Then CLK changes to ‘0’, and feedback is equal to ‘1’. X switches to ‘0’ and pull up Y to ‘1’. The out keeps ‘0’ as previous state. In the last state, both CLK and D are equal to ‘1’. X and Y keeps the value as previous state. The out is pulled down to ‘0’ and system returns to the initial state. Therefore, the system output frequency is half of the input frequency.

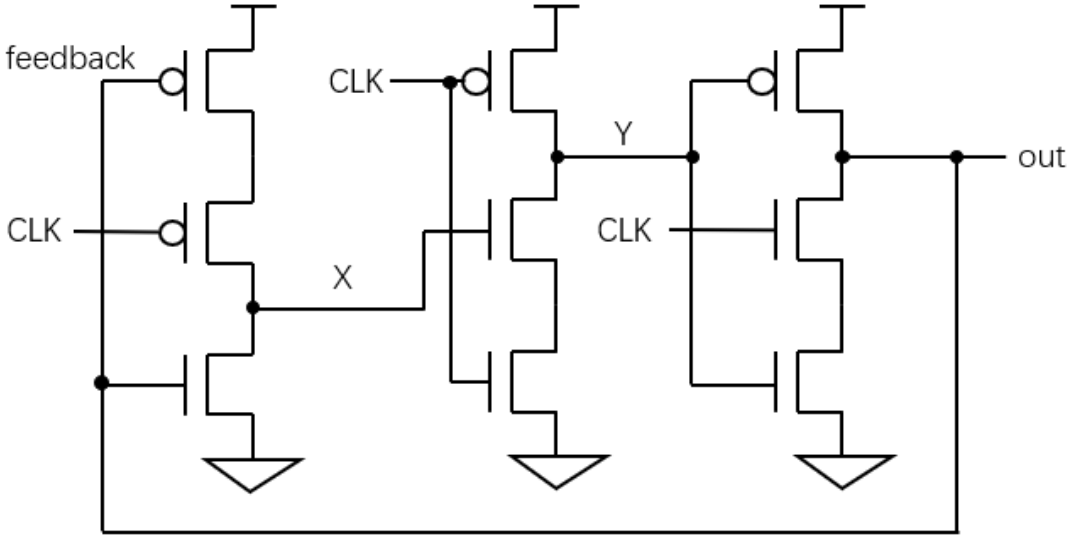

Fig 9.2.7 Schematic of single phase clock flip-flop

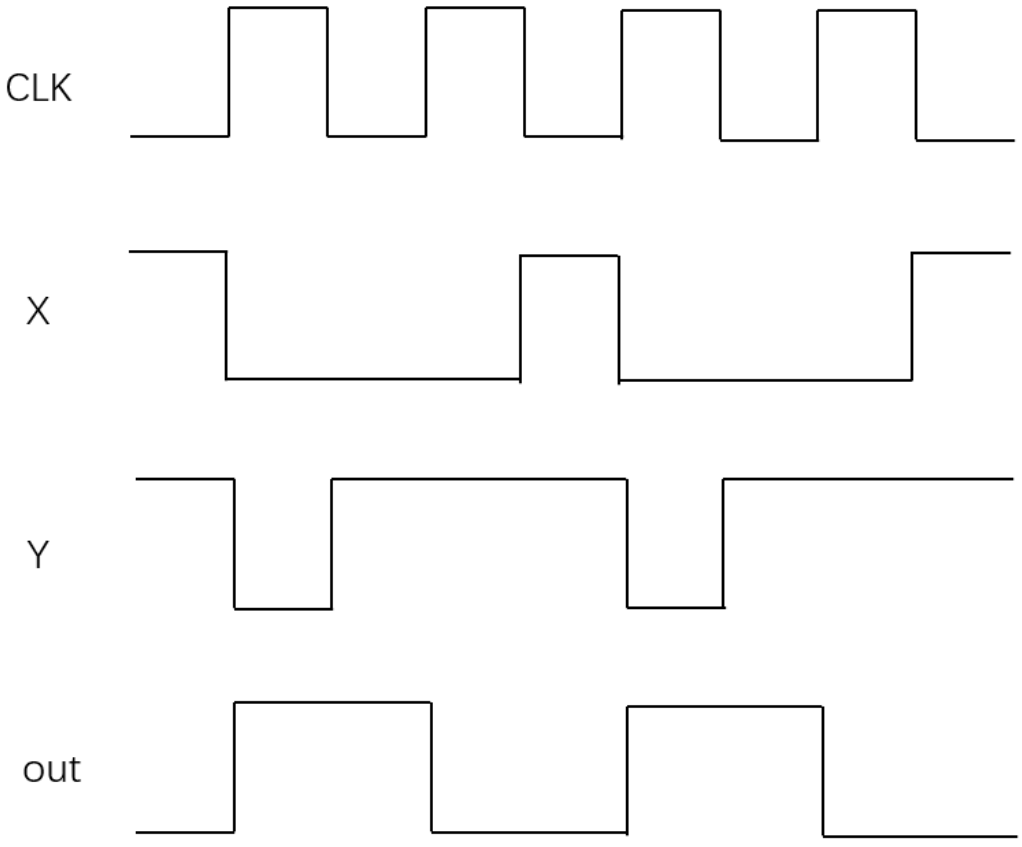

Fig 9.2.8 Operation theory of divide-by-2 circuit

9.3 Simulation Result

The proposed PLL system and its sub-circuits are designed and simulated in Cadence using 90nm CMOS technology.

From Fig 9.3.1, the minimal time difference between two input signals that PFD can differentiate is 500 ps. The average power consumption of this stage is 3.5 μW with 50 MHz input frequency. Fig 9.3.2 is the schematic of proposed quadrature phase output VCO with buffer connected at output node.

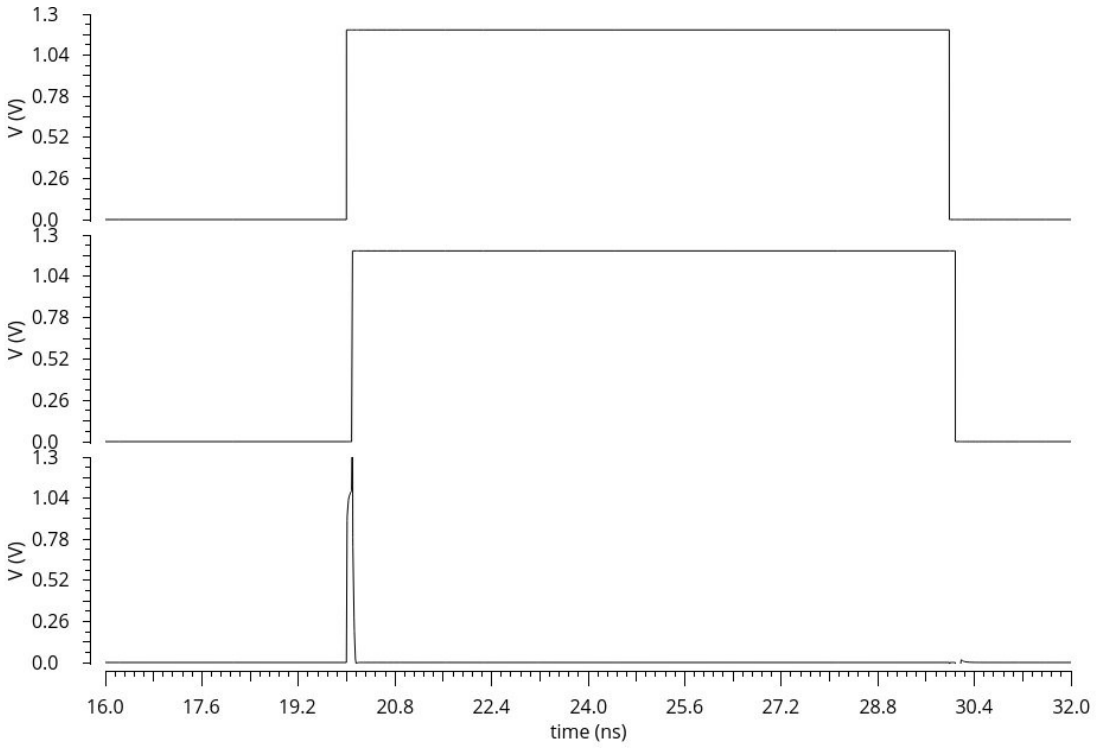

Fig 9.3.1 Simulation result of PFD with 500 ps time difference between two input signals

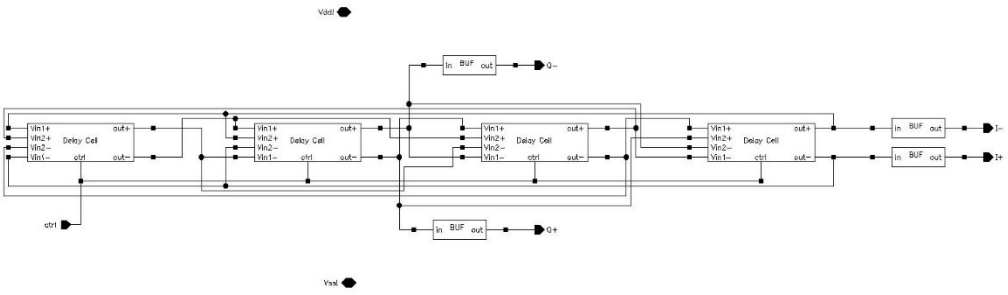

Fig 9.3.2 Schematic of proposed VCO with quadrature phase output and buffers

The oscillation frequency is 5 GHz to satisfy the receiver LO specification, and Fig. 9.3.3 demonstrate the waveform of each output node with quadrature phases. All the plots maintain 50% duty cycle with 0 V to 1.2 V full scale swing, and the average power consumption is rated as 8.67 mW.

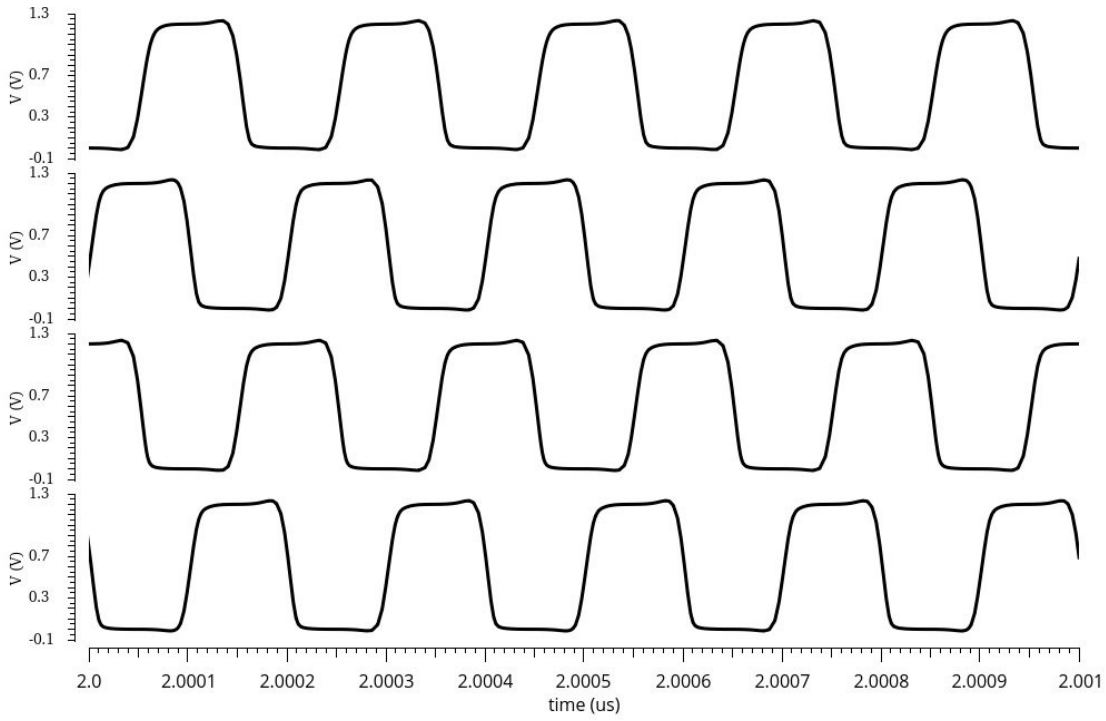

Fig 9.3.3 Simulation result of proposed VCO with I and Q outputs

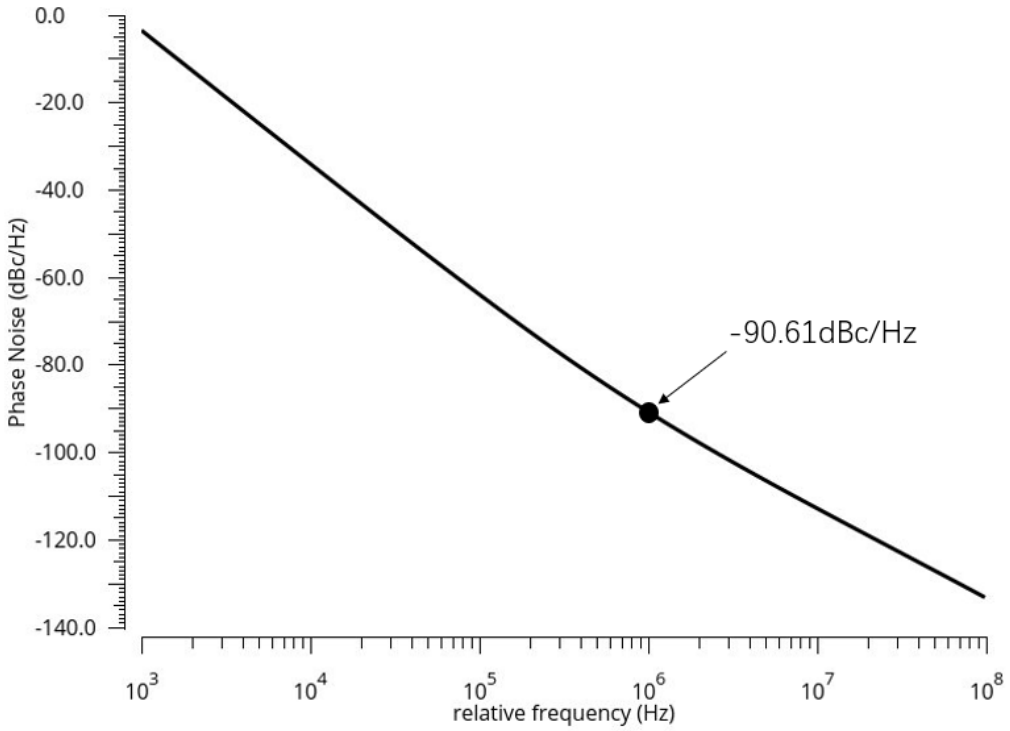

Fig 9.3.4 Phase noise of proposed VCO with 5 GHz operating frequency

Fig 9.3.4 shows the phase noise performance evaluated by Cadence RF with 5 GHz operating frequency. At 1 MHz point, the phase noise is -90.61dBc/Hz, which is acceptable for ring oscillator architecture.

The gain of VCO (K_{VCO}) is equal to 3.8 GHz/V with simulation result. Substitute this numbers with all the known value introduced in section 9.2.3 into Eq 9.2.4, the bandwidth is calculated as $4.04*10^6$ rad/s. Plug the bandwidth result along with C_z into Eq 9.2.3, the R_z value is equal to 35 KΩ when the entire loop has the quickest stabilization time. C_P value is much less than C_Z, and it is set to 500 fF in the final loop filter design.

The completed PLL schematic is shown in Fig 9.3.5, and the reference signal is set to be 39.0625 MHz, as this value is available for commercial crystal oscillator and equal to 5 GHz divided by 128.

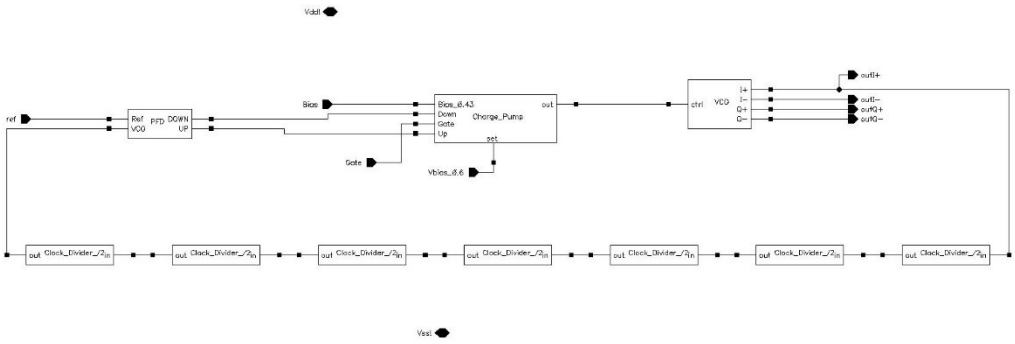

Fig 9.3.5 Schematic of PLL with sub-circuit blocks

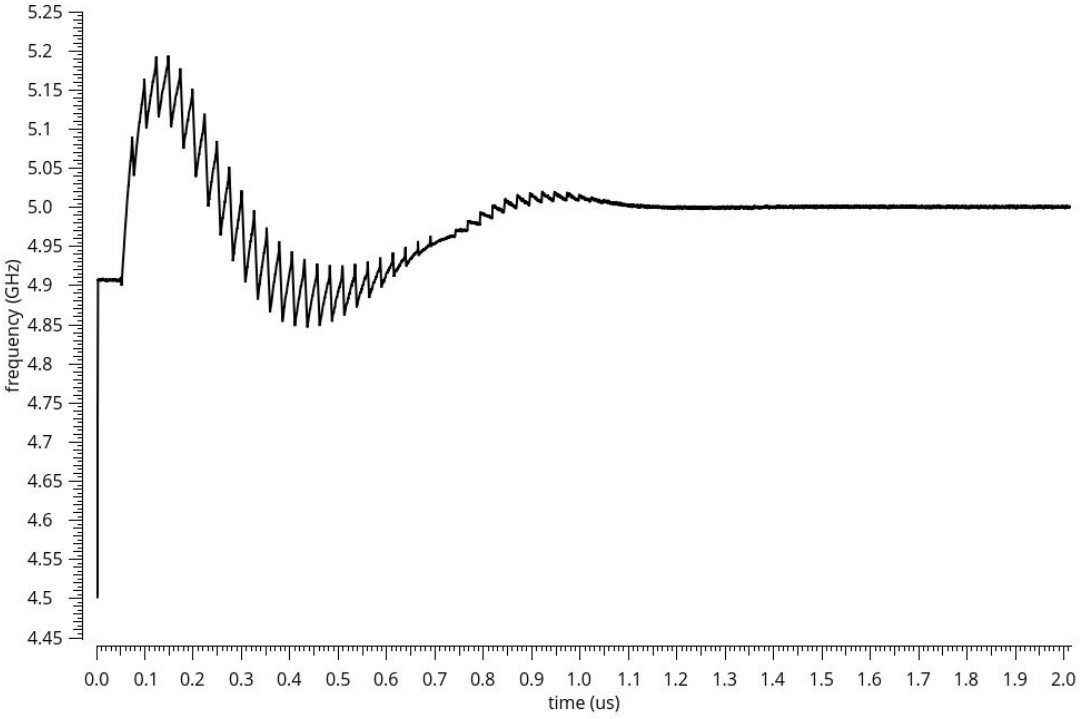

Fig 9.3.6 Frequency response of proposed PLL system.

From the simulation result in Fig 9.3.6, the designed PLL outputs 5 GHz signal with stabilization time less than 1.2 μs. The average power consumption of this PLL design is 8.67 mW.

9.4 Conclusion

In this section, a PLL system is presented to supply 5 GHz signals to receiver as LO source. Such PLL uses conventional architecture and consisted of PFD, charge pump, VCO, and dividers. To accommodate the area efficiency purpose of this dissertation, a ring oscillator structure based VCO is employed to avoid the usage of on-chip inductor. Meanwhile, such VCO provides quadrature phase outputs for Hartly architecture specification and relatively low phase noise of -90.61dBc/Hz at 1 MHz. The proposed PLL features fast settling time and good stability for maintaining 5 GHz signal with 50% duty cycle. The average power consumption of entire system is 8.67 mW which is reasonable considering its 5 GHz operating frequency.

X. Analog 90 Degree Phase Shifter

10.1 Introduction

As discussed in the first chapter, the key component of building Hartley system is the 90 degree phase shifter [52]. By having this stage placed in $sin(\omega_{LO}t)$ path, the signals generated from two paths have differential IF component and identical image part. Thus, the image signal can be easily removed by subtracting two signals using a differential amplifier. However, to have a good image rejection performance in Hartley architecture, the 90 degree phase shifter must provide good phase shifting accuracy and minimum gain mismatch error. Moreover, this phase shifter needs to be designed with the consideration of power and area efficiency to fit entire receiver design objectives proposed in this dissertation.

To satisfy the specification listed above, a 90 degree phase shifter using RC-CR architecture is introduced in this chapter. The gain mismatch compensation is achieved by employing active resistor that can alternate frequency response at output node. This feature guarantees two signals with 90 degree phase difference having the same amplitude across entire system bandwidth.

10.2 RC-CR Network

The RC-CR network shown in Fig 10.2.1 is built by two signal paths with active resistor and capacitor connected in series. The output signals can be expressed as:

$$V_{out1} = \frac{R}{1+\frac{1}{j\omega C}} = \frac{j\omega RC}{1+j\omega C} \tag{10.2.1}$$

$$V_{out2} = \frac{\frac{1}{j\omega C}}{1+\frac{1}{j\omega C}} = \frac{1}{1+j\omega C} \tag{10.2.2}$$

The phase of these two signals are:

$$\angle V_{out1} = \frac{\pi}{2} - \tan^{-1} \omega RC \tag{10.2.3}$$

$$\angle V_{out2} = -\tan^{-1} \omega RC \tag{10.2.4}$$

Comparing Eq 10.2.3 and 10.2.4, the phase difference between two output nodes is 90 degree over all frequency. Moreover, these two paths of the circuitry are equivalent to low-pass and high-pass filter, respectively. Since the 3dB down cutoff frequency (f_C) of RC circuit has phase of 45 degree, the two output signals can have the same amplitude at f_C point with 90 degree phase difference as shown in Fig 10.2.2. The 3dB down cutoff frequency (f_C) of V_{out1} and V_{out2} are equal to:

$$f_C = \frac{1}{2\pi RC} \tag{10.2.5}$$

If capacitor is set to be 2 pF, then the resistance of each path needs to be 318 Ω to place the f_C at 250 MHz frequency as system IF center frequency.

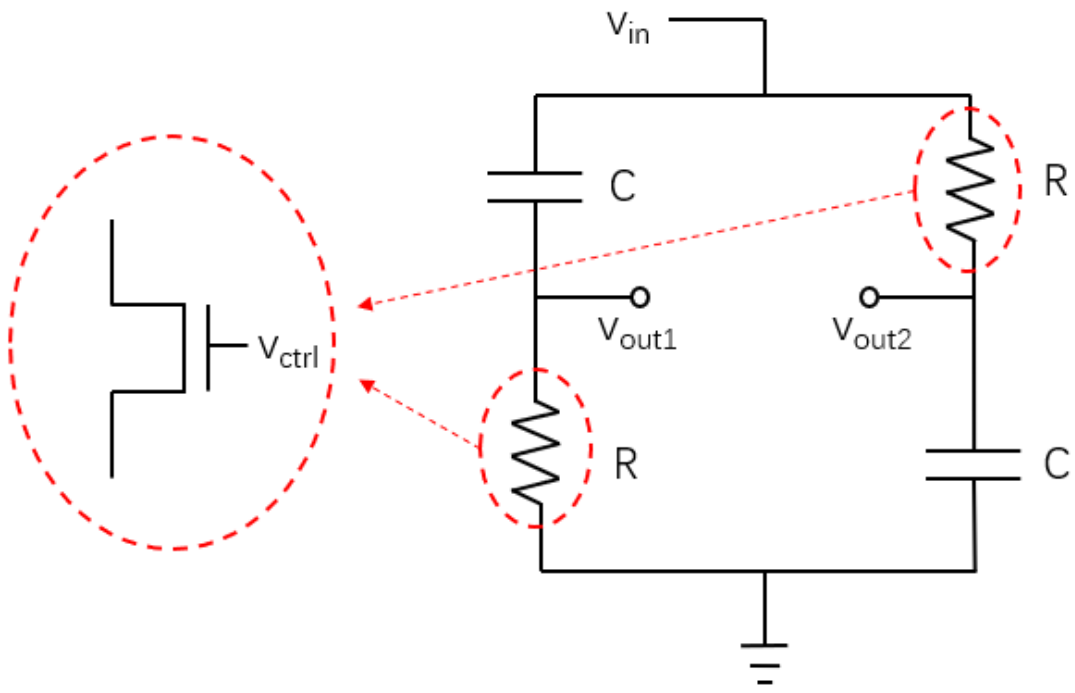

Fig 10.2.1 RC-CR Network with adjustable resistor (active load)

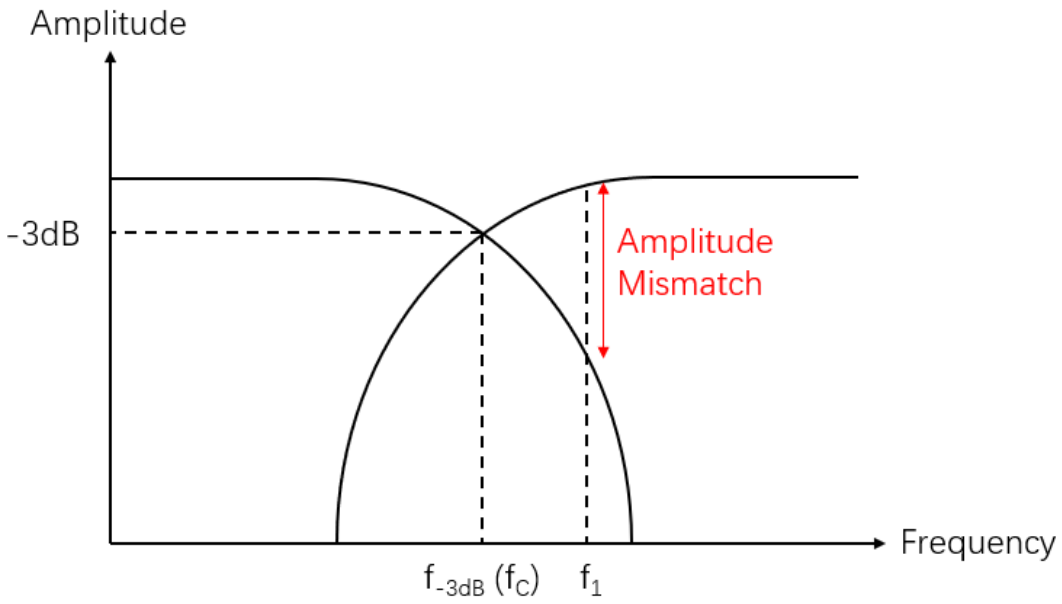

Fig 10.2.2 Frequency response of high pass and low pass filter with gain mismatch phenomenon of phase shifter

However, if input signal frequency changes, the amplitude of two output becomes disparate, and this gain mismatch degrade the quality of system image rejection. To address this issue, either resistor or capacitor in circuitry must be capable of varying its value without changing physical geometry. In this dissertation, this feature is achieved with active resistor built by CMOS transistor and controlled by gate voltage.

For transistor working in linear region, the drain to source resistance for N-type MOSFET can be estimated as below:

$$I_D = \mu * C_{ox} * \frac{W}{L} * (V_{GS} - V_T) * V_{DS} \tag{10.2.6}$$

In Eq 10.2.6, μ is the mobility of electronics and C_{ox} is the oxide capacitance in transistor. The W and L describe the width and length of transistor and V_T is the threshold voltage that can turn on the transistor. Noted that, in Eq 10.2.6, the gate to source voltage V_{GS} must be greater than V_T to allow current I_D flowing through transistor. Besides, in order to operate transistor in linear region, the drain to source

voltage V_{DS} needs to be smaller than V_{GS} - V_T. Thus, the equivalent resistance between drain and source nodes can be derived as:

$$R_{DS} = \frac{V_{DS}}{I_D} = \frac{1}{\mu * C_{ox} * \frac{W}{L} * (V_{GS} - V_T)} \tag{10.2.7}$$

It can be seen that the effective resistance of transistor is able to be varied by changing the gate voltage. Therefore, the gain calibration can be achieved by adjusting gate voltage to compensate the gain mismatch error at different input frequency.

10.3 90 Degree Phase Shifter Simulation Results

The 90 degree phase shifter with self-calibration system is built and simulated in 90nm technology. The schematic diagram is demonstrated in Fig 10.3.1 with built-in input blocking capacitor to set the signal offset value. The testing frequency band is the down-converted IF frequency band from 170 MHz to 330MHz. In the initial setup, the 250 MHz input signal sending into phase shifter creates two output signals with same frequency and amplitude but 90 degree phase difference as shown in Fig 10.3.2.

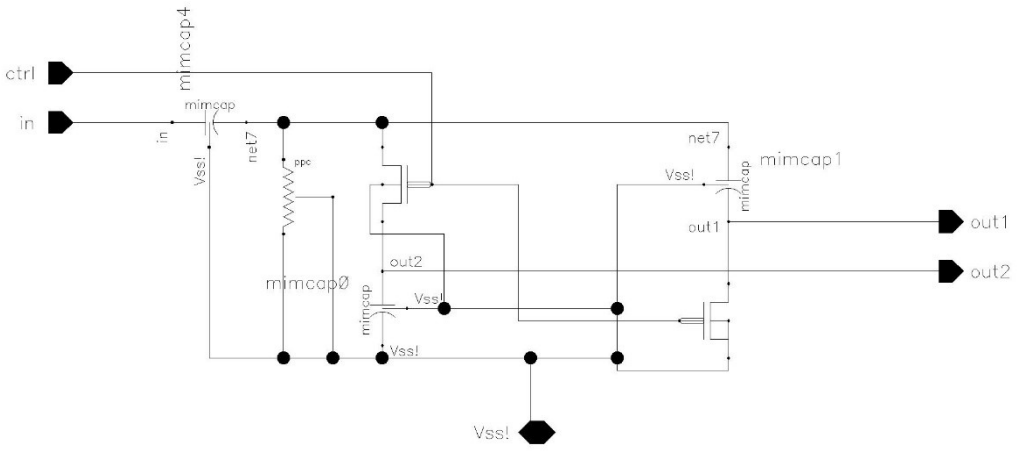

Fig 10.3.1 Schematic diagram of 90 degree phase shifter using RC-CR network.

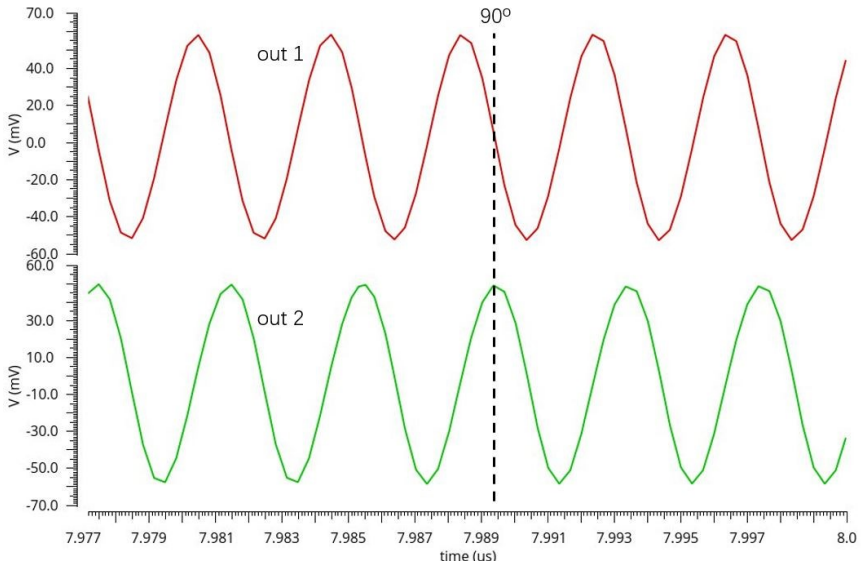

Fig 10.3.2 90 degree phase shifter two outputs waveforms at 250 MHz

Fig 9.4.3 and Fig 9.4.4 demonstrate the waveforms before and after calibration when input frequency is 170 MHz and 330 MHz, respectively. In these two simulation results, the input amplitude is 100 mV. However, due to the frequency change, the output signals amplitude difference is 20.6 mV for 170 MHz case and 15.5 mV for 330 mV case before calibration. After adjusting the gate voltage of active load transistor, the amplitude difference between two output signals are 0.5 mV for both 170 MHz and 330 MHz input frequency.

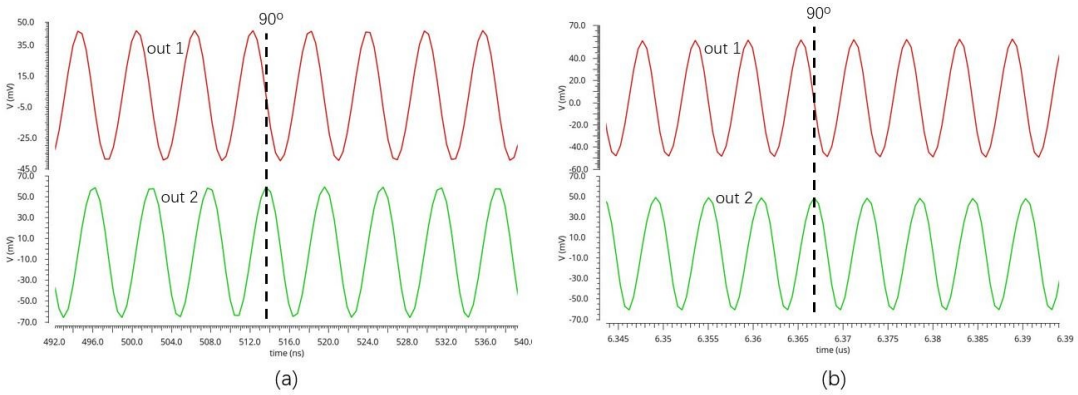

Fig 10.3.3 90 degree phase shifter two outputs waveforms at 170 MHz: (a) Before calibration (b) After calibration

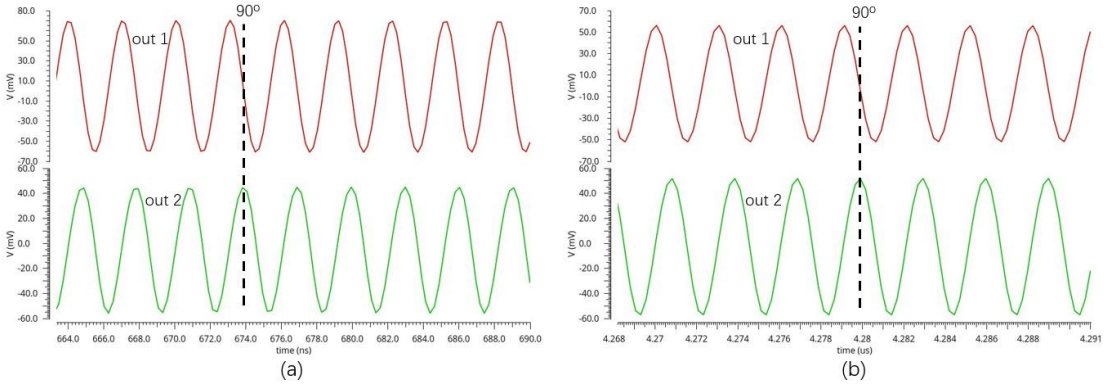

Fig 10.3.4 90 degree phase shifter two outputs waveforms at 330 MHz: (a) Before calibration (b) After calibration

Table 10.3.1 90 Degree Phase Shifter Output Amplitude Difference

Input Frequency	Control Voltage	Amplitude Difference between 2 Outputs
250 MHz	590 mV	0.05 mV
170 MHz	590 mV	20.6 mV
	500 mV	0.5 mV
330 mV	590 mV	15.5 mV
	670mV	0.5 mV

From Table 10.3.1, the two output signals of phase shifter can have minimum gain mismatch error with proper control voltage loaded.

10.4 Conclusion

In this chapter, a 90 degree phase shifter using RC-CR network technique is designed and simulated with 90 nm technology. To have the same amplitude of 2 output signals among demanding frequency band, the CMOS transistor is employed as active resistor in the circuit and its resistance can be tuned by changing gate voltage. Therefore, the gain mismatch error between two output nodes created by different input frequency

is compensated by adjusting the active resistance. The simulation results indicate the designed phase shifter can maintain 90 degree difference and same amplitude between two output signals within the frequency band from 170 MHz to 330 MHz. The average power consumption of the phase shifter system is 10.19 μW when input signal has 100 mV amplitude and 250 MHz frequency.

XI. System Performance

11.1 Performance Comparison between Hartley and Weaver System

In this section, the Weaver and Hartley systems are implemented and simulated with Cadence using 90 nm technology. Both architectures are performed the noise figure, image rejection ratio, and power consumption simulations to evaluate the system performance and decide which design fits the entire front end receiver better. Detailed simulation results are presented in following sub-sections.

11.1.1 Hartley System Simulation Results

The proposed Hartley system schematic diagram is demonstrated in Fig 11.1.1, and it contains the IQ paths to achieve image rejection function at the final output node with the help of 90 degree phase shifter. The noise figure simulation plot is shown in Fig 11.1.2 with 40.14 dB at selected band center frequency of 5.25 GHz. The power consumption is measured as 6.974 mW with 0.1 mV input amplitude.

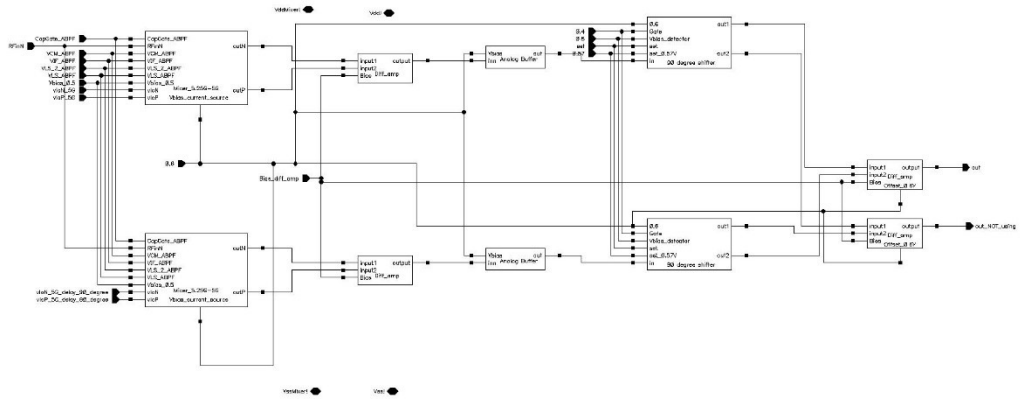

Fig 11.1.1 Schematic diagram of proposed Hartley system.

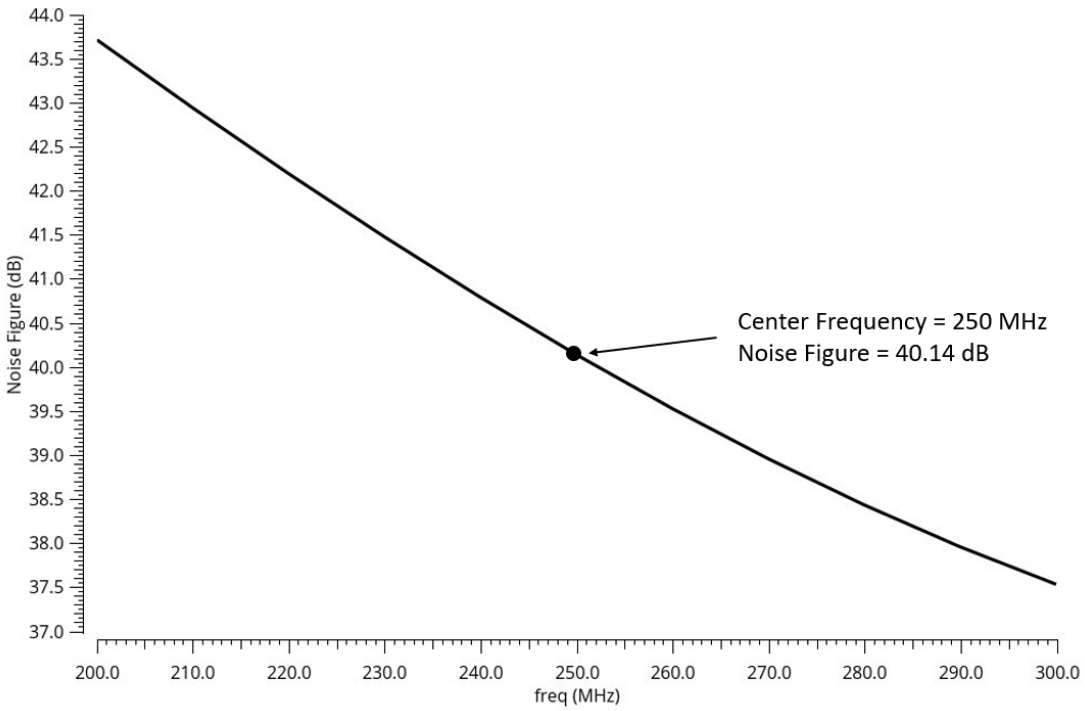

Fig 11.1.2 Noise figure plot of proposed Hartley system.

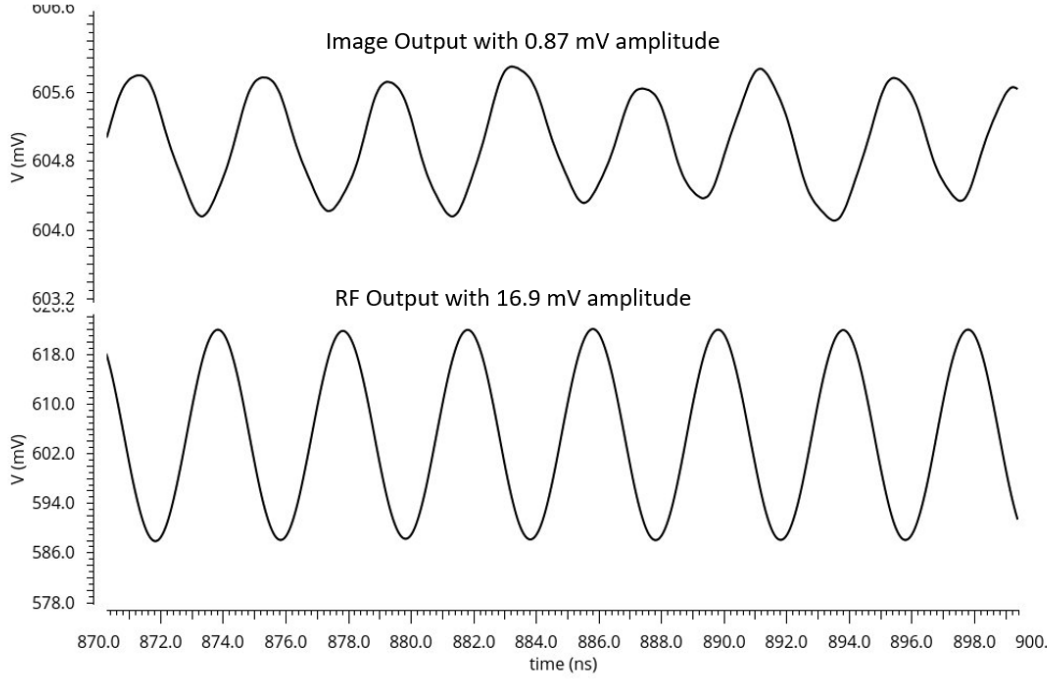

Fig 11.1.3 Hartley System output waveforms generated by RF and Image signals.

The Image Rejection Ratio (IRR) is defined as:

$$IRR\ (dB) = 20\log_{10}\frac{V_{outRF}}{V_{outImage}} \tag{11.1.1}$$

In Eq 10.1.1, V_{outRF} is the amplitude of output signal down-converted by RF input, and $V_{outImage}$ is the amplitude of output signal up-converted by image input. Using the transient analysis results shown in Fig 11.1.3, this IRR value can be calculated as 25.76 dB.

11.1.2 Weaver System Simulation Results

Fig 11.1.4 shows the schematic diagram of designed Weaver system. As stated in chapter 8, this dual frequency conversion architecture is transforming the 5.25 GHz RF signal into 750 MHz temporary IF signal by 4.5 GHz LO signal first, then uses second LO source with 500 MHz frequency to further down-converted the first stage output to 250 MHz as the final IF signal.

The noise figure is 52.24 dB for the Weaver system and simulation plot is shown in Fig 11.1.5. The average power consumption is measured as 16.15 mW when input signal is set to 0.1 mV amplitude. These two numbers are quite large comparing to the results of Hartley design due to the extra mixers and active filters.

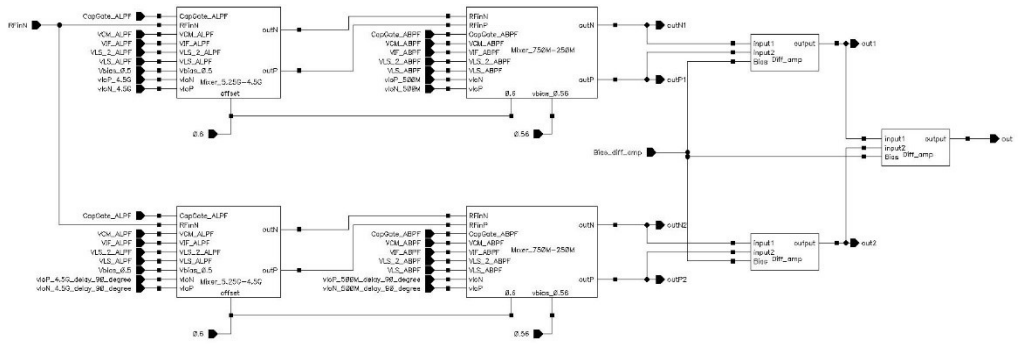

Fig 11.1.4 Schematic diagram of designed Weaver system

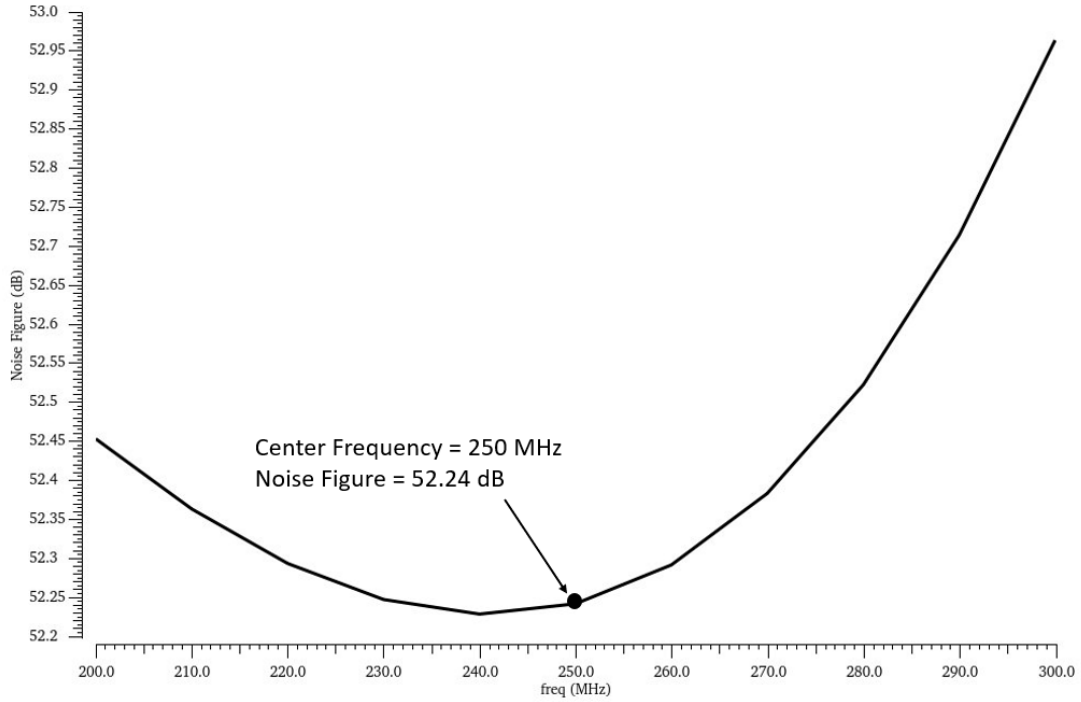

Fig 11.1.5 Weaver system noise figure.

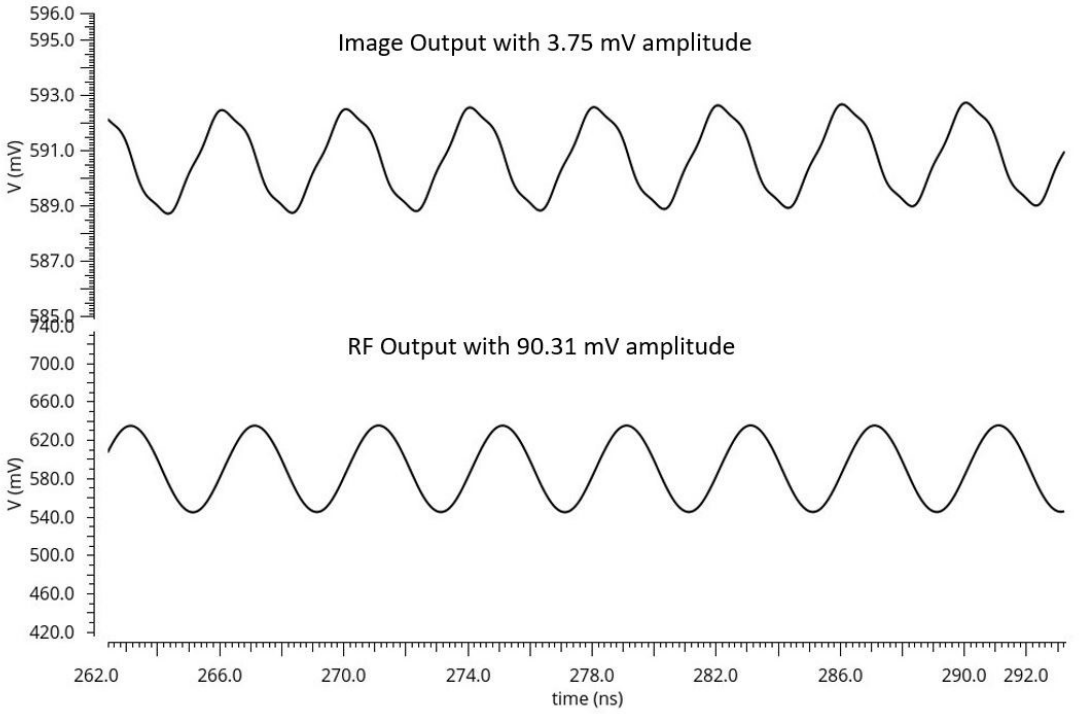

Fig 11.1.6 Weaver system output waveforms generated by RF and Image signals.

The input frequency of measuring image rejection ratio are 5.25 GHz and 4.75 GHz. Both transient analysis results are presented in Fig 11.1.6, and the rejection ratio can be calculated as 27.63 dB using Eq 11.1.1.

Through the simulation results, Weaver system provides better image rejection ratio than Hartley design due to its two-stage frequency conversion architecture. However, with less active circuits involved in the design, the Hartley system offers better noise performance and low power consumption which are the key parameters of wireless front end implementation. In the following section, the proposed receiver design is implemented and simulated with Hartley system.

11.2 Proposed Heterodyne plus Hartley Receiver Simulation Results

The proposed receiver system combined Heterodyne and Hartley architecture is designed and simulated in Cadence using 90 nm technology. System schematic diagram is presented with circuit blocks in Fig 11.2.1 and the detailed implementation of each stage has been discussed in previous chapters.

The schematic simulation results of proposed receiver are summarized in Table 11.2.1 with 5.25 GHz input frequency.

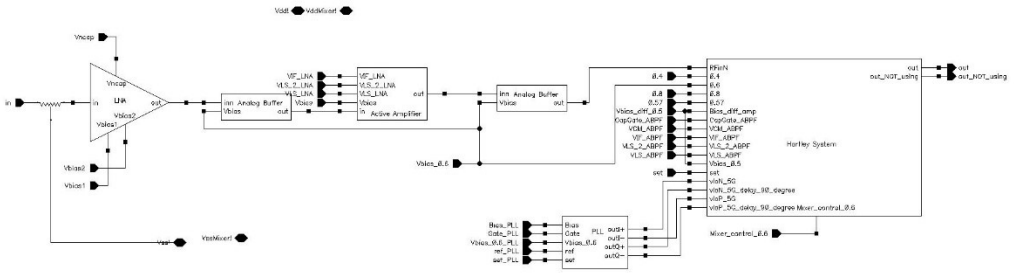

Fig 11.2.1 Proposed receiver schematic diagram.

Table 11.2.1 Proposed Receiver Simulation Results

Parameter	Simulation Results
Gain (dB)	45.8
Bandwidth (MHz)	200
Input Sensitivity (dBm)	-90
Noise Figure (dB) (without PLL)	10.72
Image Rejection (dB)	35.63
Power Consumption (mW)	28.42
Maximum Input Power (dBm)	-50

The minimum input power that the receiver can detect, and transfer is -90 dBm, which satisfied the input sensitivity requirement in 802.11ac standard (-73 dBm). Noise figure value listed in the table is simulated at system highest gain mode. Since the RF stage circuits (LNA+AIBPF) are implemented with low noise and high gain feature, the entire front-end noise is suppressed even the IF stage employs two mixers and noisy. This parameter is calculated based on Eq 2.2.4 with the Noise Figure of RF section and Hartley system, and the simulation results is contained in Fig 11.2.2 and 11.1.2. However, even such high gain design in RF phase can pick weak signal (-90 dBm) but it also limits the input power range, and the maximum unsaturated input power of proposed receiver design is -50 dBm.

Image rejection ratio is simulated with both RF (5.25 GHz) and Image (4.75 GHz) signals sending into receiver with same amplitude. The output of these two frequency signal is shown in Fig 11.2.3, and proposed receiver image rejection is calculated as 35.63 dB with Eq 11.1.1. Even though, this result is not comparable with some latest publications, considering the proposed receiver using IF band and rejecting image signal at analog phase, this number is acceptable. Moreover, Hartley architecture is implemented based on I-Q signal format, so these two signals can also be used to perform image rejection at digital phase to improve the rejection ratio.

From Fig 11.2.4, the minimum and maximum power input result in output amplitude of 11.5 mV and 195 mV, respectively. These two values can be converted as 4 bits and 8 bits using Eq 2.2.3 under the assumption of ADC in [25] connected to the system. The average power consumption of proposed receiver is 28.42 mW.

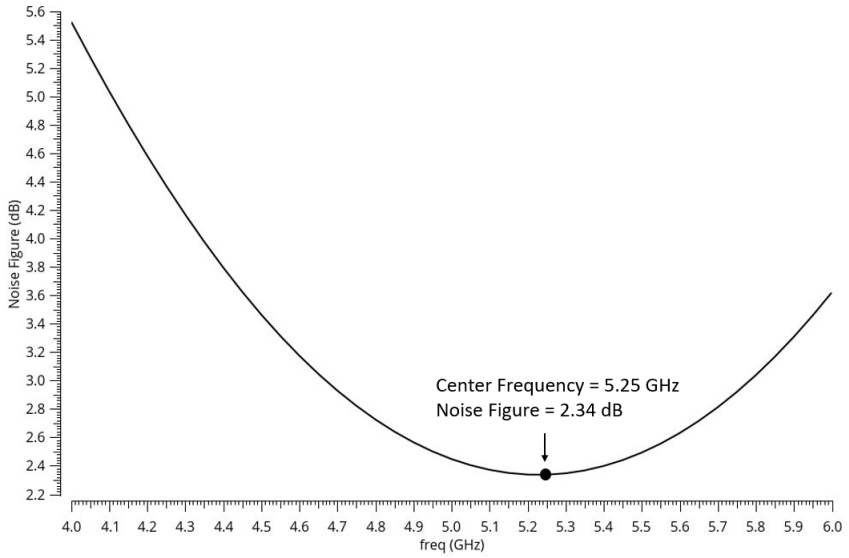

Fig 11.2.2 Noise figure of receiver RF section circuits.

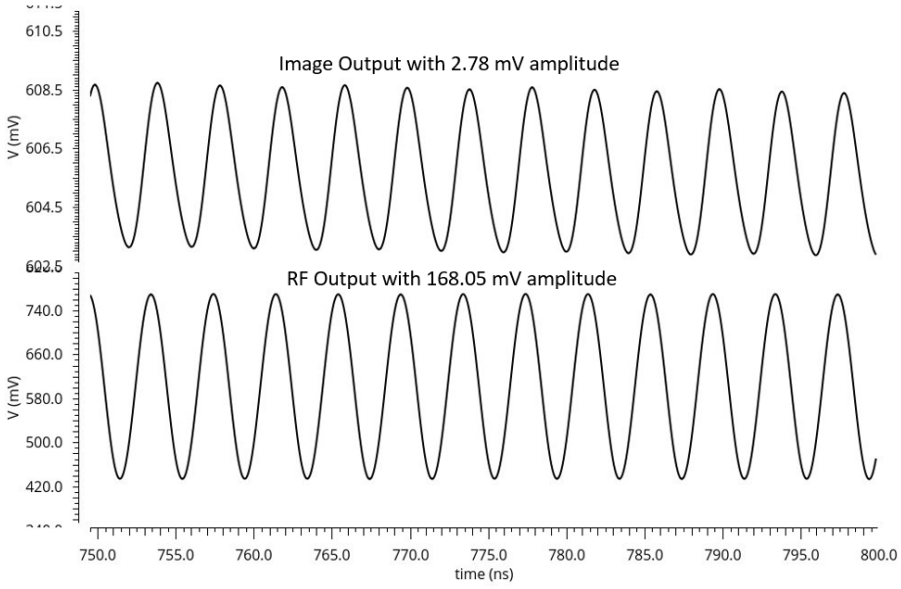

Fig 11.2.3 Proposed receiver output plots of RF (5.25 GHz) and image (4.75 GHz) input signal with image rejection of 35.63 dB.

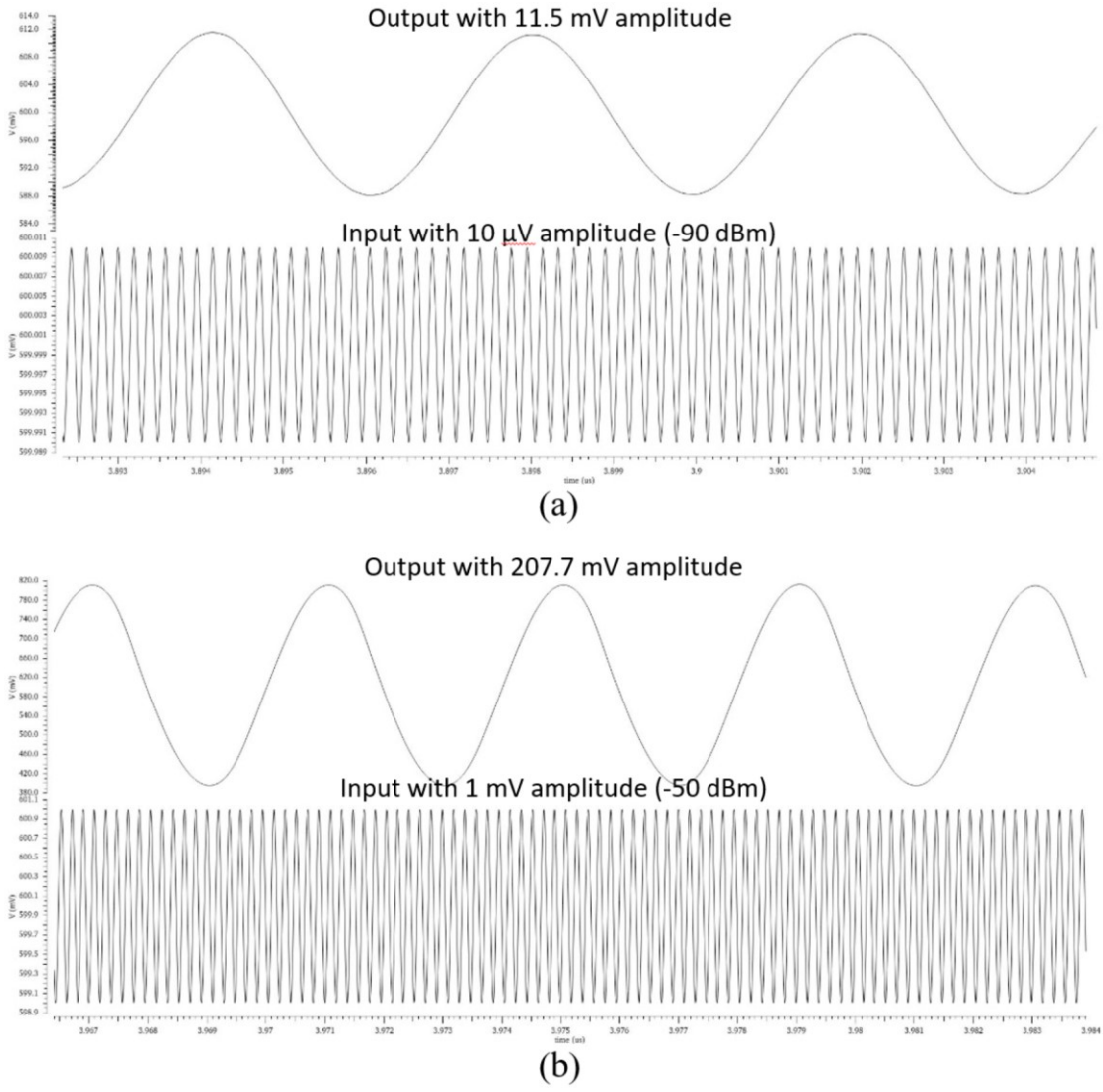

Fig 11.2.4 Transient simulation results of proposed receiver design: (a) input power of -90 dBm; (b) input power of -50 dBm.

11.3 Conclusion

In this chapter, two popular analog image rejection system: Hartley and Weaver have been designed and simulated. Simulation results indicate that even though the Weaver design provides better image rejection, the Hartley architecture is more suitable for mobile WLAN applications, as it has low noise and low power consumption benefits. A CMOS Hartley receiver is built with all circuits mentioned in previous chapters and

tested to verify the entire front-end chain performance. The proposed receiver is compatible with 802.11ac standard, and it features low noise, high input power sensitivity, and potential small area consumption.

XII. Conclusion and Future Works

12.1 Conclusion

In this dissertation, a CMOS receiver design compatible with 802.11ac WLAN standard is presented. This system uses active inductor to replace conventional on-chip passive inductor for area saving and performance improving purpose. Hartley architecture is employed in proposed receiver to reject image signal and enhance extracted information quality.

12.2 Major Contributions

- Designed active inductor and active inductor-based band pass filter with better quality factor and on-chip area efficiency than conventional passive design.
- Developed a post-fabrication calibration system that can detect process variation and automatically compensate the center frequency shifting error of active inductor-based band pass filter.
- Designed sub-circuits of calibration system (Peak detector, Analog buffer, etc).
- Designed a Phase Locked Loop system that outputs quadrature phase 5 GHz signal as LO source of mixer.
- Designed a receiver chain that suitable for mobile WLAN application, and embedded active inductor-based band pass filter in the system to improve area efficiency and quality factor.
- Combined Heterodyne and Hartley architecture to perform image rejection in analog design phase.

12.3 Future work

12.3.1 Calibration System Optimization

The calibration system introduced in Chapter VII still has room to be improved. First, the circuitry needs off-chip instrument to deliver reference signals for system operating. This requirement can increase the complexity and cost of calibration process, and the chip needs to provide two extra pins for only compensation purpose. Second, the calibration system cannot correct the center frequency shifting error of filter when compared signals amplitude difference is lower than system sensitivity at extreme process corner. For future work, a built-in PLL can be used to generate the reference signal on-chip and construct a fully-automatic calibration system for active inductor based band pass filter. A better comparator can be designed that maintains fine resolution at different process corner.

12.3.2 Active Inductor Based Band Pass Filter Gain Calibration

In this dissertation, a center frequency error compensation system is design to overcome process variation for active inductor based band pass filter. However, the gain deviation due to process variation is another drawbacks that prevent the wide-scale use of active filter. For the future work, a hybrid system that contains both frequency and gain calibration can make the active band pass filter more attractive for on-chip circuit design.

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